

Application Note

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FASTBIT FB100A

BER ANALYSIS USING FRAMED DATA



Flexible, programmable framing allows the test engineer to make BER tests on payloads within complex framing structures with ease.

For the very latest specifications visit www.aeroflex.com

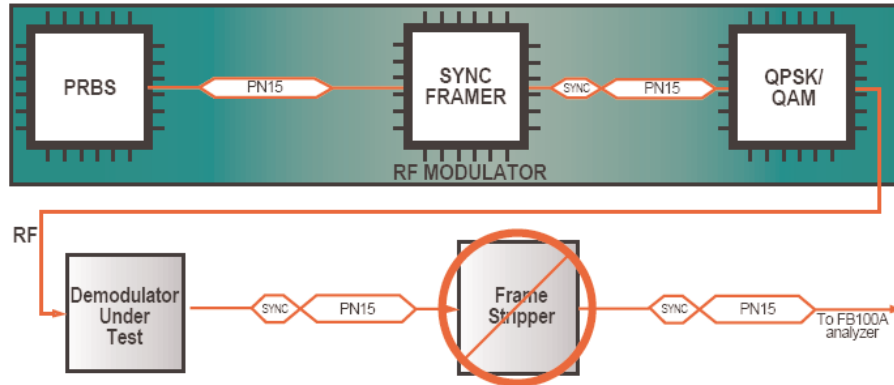


Figure 1. Typical setup for DBV, DOCSIS, DSS RF demodulator BER test

TECHNICAL HIGHLIGHTS

- Test engineers can now make BER measurements on framed data structures without fabricating a frame stripper board
- "Burst" clock and data streams do not have to be re-timed and smoothed prior to BER analysis
- Modulator - generated frames can be used for test purposes
- Test data does not have to originate in the BERT pattern generator
- Very quick synchronization to patterns with low data rates with long PRBS patterns

RELATED APPLICATION NOTES

- AUTOMATED BER PLOTS USING FB100A BER TEST SYSTEM AND INTEGRATED NOISE AND IMPAIRMENT MODULE
- MEASURING BER OF DEVICES WITH UNIQUE SERIAL AND PARALLEL INTERFACES
- BER TEST TIME OPTIMIZATION

BERT SYNCHRONIZATION ISSUES

Modern RF digital transmission of video, audio and data requires the use of data frames as defined by several standards; i.e. DVB, DOCSIS, DSS, etc. For example, MPEG transport streams consist of a 47h sync byte in front of 187 bytes of payload data. With this type of frame structure, it is impossible for traditional BERTs to acquire synchronization. An external frame stripper must be added to remove the sync byte and smooth the data to provide the continuous Pseudo-random Binary Sequence (PRBS) input that they require.

Some BERTs attempt to solve this problem by concatenating framing with a software generated PRBS into a long sequence of pre-defined bits. This approach fails, particularly if the test system uses a PRBS not generated by the BERT generator, but rather by a test PRBS internal to the modulator. In many cases the engineers find themselves having to wait several minutes or more for the BERT to acquire sync. Thus, the instant feedback often needed for modulator evaluation and debug is lost.

INSTALOK™ - FAST SYNCHRONIZATION ON COMPLEX FRAMES

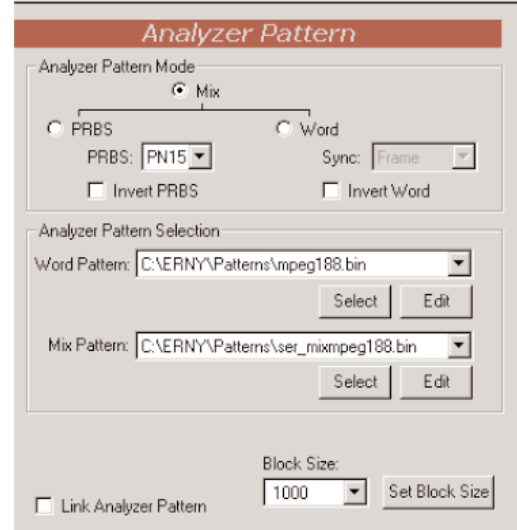
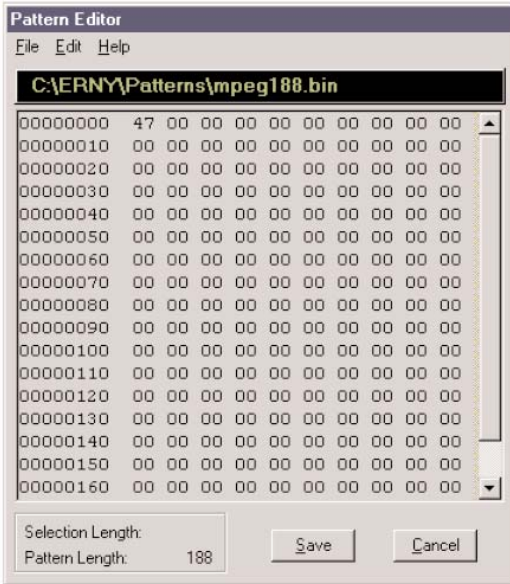
The FB100A uses a unique, two step synchronization process to solve this challenge. First, the BERT analyzer looks for a user-defined Frame Sync Word (FSW). Once the FSW is found, the analyzer attempts to synchronize to the PRBS payload data using the feed-forward technique.

By taking this two step approach, the position of the framing pattern with respect to the payload is immaterial. Even if the pattern is generated by a source other than the BERT generator, the analyzer still synchronizes. Test patterns generated by a test modulator are no challenge, regardless of the data rate.

SETTING UP THE MEASUREMENT

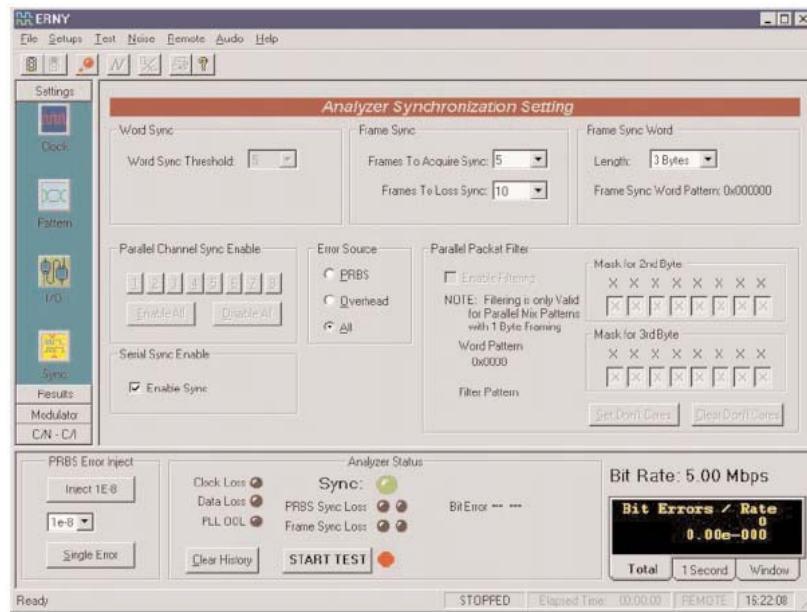
STEP 1

Select "Patterns" from the vertical menu bar on the left. Select "Mix" in the Analyzer Pattern editor screen. Determine the PRBS code used in the received frame payload. Use the Word Pattern and Mix Pattern hex editor to program the expected frame overhead value and length. Zeros programmed in the mix pattern MSB will select data bytes from the PRBS code generator, while ones will select data from the respective byte locations of the programmable word RAM.



STEP 2

Click on the "Synchronization" icon on the vertical toolbar. Under "Frame Sync Word" select the number of bytes used at the beginning of the frame for synchronization purposes. Under "Frame Sync" you can specify the number of consecutive good frames needed to acquire sync. Five is a typical number. You can also specify the number of consecutive bad frames to transition to the "Frame Sync Loss" condition.



RUNNING THE TEST

For a manual test, click the "Start Test" command button at the bottom of the FB100A display.

For automated Eb/No measurements, refer to Application Notes:

- Automated BER plots using FB100A BER test system and integrated noise and impairment module
- BER Test Time Optimization.

CHINA Beijing

Tel: [+86] (10) 6467 2761 2716
Fax: [+86] (10) 6467 2821

CHINA Shanghai

Tel: [+86] (21) 6282 8001
Fax: [+86] (21) 62828 8002

FINLAND

Tel: [+358] (9) 2709 5541
Fax: [+358] (9) 804 2441

FRANCE

Tel: [+33] 1 60 79 96 00
Fax: [+33] 1 60 77 69 22

GERMANY

Tel: [+49] 8131 2926-0
Fax: [+49] 8131 2926-130

HONG KONG

Tel: [+852] 2832 7988
Fax: [+852] 2834 5364

INDIA

Tel: [+91] 80 5115 4501
Fax: [+91] 80 5115 4502

KOREA

Tel: [+82] (2) 3424 2719
Fax: [+82] (2) 3424 8620

SCANDINAVIA

Tel: [+45] 9614 0045
Fax: [+45] 9614 0047

SPAIN

Tel: [+34] (91) 640 11 34
Fax: [+34] (91) 640 06 40

UK Burnham

Tel: [+44] (0) 1682 604455
Fax: [+44] (0) 1682 662017

UK Stevenage

Tel: [+44] (0) 1438 742200
Fax: [+44] (0) 1438 727601
Freephone: 0800 282388

USA

Tel: [+1] (316) 522 4981
Fax: [+1] (316) 522 1360
Toll Free: 800 835 2352

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www.aeroflex.com
info-test@aeroflex.com



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