3020A, 3020C, 3021C, 3025, 3025C, 3026C
(3020 Series)
Digital RF Signal Generator PXI Modules

User Manual

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About this manual

This manual explains how to set up and configure an Aeroflex 3020A, 3020C, 3021C, 3025, 3025C or 3026C digital RF signal generator PXI module. Where necessary, it refers you to the appropriate installation documents that are supplied with the module.

Please note: this manual applies only when the instrument is used with the supplied software.

This manual provides information about how to configure the module as a stand-alone device. However, one of the advantages of Aeroflex 3000 Series PXI modules is their ability to form versatile test instruments, when used with other such modules and running 3000 Series application software.

Getting Started with afSigGen (supplied on the CD-ROM that accompanies each module (see Associated documentation)) explains how to set up and configure a 3020 Series RF signal generator with a 3010 Series RF synthesizer module. Using the signal generator soft front panel and/or dll or COM object supplied, the modules form an instrument that provides the functionality and performance of an integrated, highly-specified signal generator, but with the adaptability to satisfy a diverse range of test or measurement requirements.

Intended audience

Engineers who need accurately-generated signals in the MF, HF, VHF and UHF spectra.

This manual is intended for first-time users, to provide familiarity with basic operation. Programming is not covered in this document but is documented fully in the help files that accompany the drivers and associated software on the CD-ROM.

Driver version

This PXI RF module is designed to be used with the latest software driver version supplied on the Aeroflex 3000 Series PXI Modules CD-ROM, part no. 46886/028. Operation with earlier versions of driver software may not be supported.

Associated documentation

If you want to…	Refer to…
Find information about soft front panels, drivers, application software, data sheets, installation, getting started and user manuals for this and other modules in the 3000 Series	**PXI Modules CD-ROM** Part no. 46886/028 Supplied with the module
Install modules into a rack, interconnect them, power up and install drivers	**3000 Series PXI Modules Common Installation Guide** Part no. 46892/663 On the CD-ROM and at www.aeroflex.com/
Set up a populated chassis ready for use	**3000 Series PXI Modules Installation Guide for Chassis** Part no. 46892/667 On the CD-ROM and at www.aeroflex.com/
Set up and use the universal PXI application for system configuration and operation	**PXI Studio User Guide** Part no: 46892/809 On the CD-ROM and at www.aeroflex.com/

If you want to…	Refer to…
Set up and use a signal generator application for 3010 Series and 3020 Series modules	**Getting Started with afSigGen** Part no. 46892/678 On the CD-ROM and at www.aeroflex.com/
Download example source code	You can download examples of source code (written for different application development environments) from the Aeroflex website here.

Preface

The PXI concept

VXI and GPIB systems meet the specific needs of instrumentation users but are often too large and expensive for mainstream applications. PC-based instrumentation may cost less but cannot meet the environmental and operational requirements of many systems.

PXI (PCI Extensions for Instrumentation) is based on CompactPCI, itself based on the PCI standard. PCI was designed for desktop machines but CompactPCI was designed for industrial applications, and features a rugged Eurocard format with easy insertion and removal. PXI adds to the CompactPCI specification by defining system-level specifications for timing, synchronization, cooling, environmental testing, and software. While PXI extends CompactPCI, it also maintains complete interoperability so that you can use any CompactPCI-compliant product in a PXI system and vice versa. PXI also makes use of Windows software, VXI timing and triggering, and VXIplug&play instrument drivers to provide powerful and affordable systems.

PXI Express now integrates PCI Express into PXI, providing up to 6 Gbyte/s backplane bandwidth and up to 2 Gbyte/s slot bandwidth. PXI Express maintains backwards compatibility with PXI, providing software compatibility and hardware compatibility with hybrid slots and hybrid systems.

Hybrid slot compatibility

PXI chassis that provide hybrid slots can accept both PXI Express modules and hybrid-compatible PXI modules. Hybrid-compatible PXI modules have a ‘missing’ section of connector (see Fig. 1), which allows them to be inserted into both hybrid slots and standard PXI-1 slots.

Because of the reduced connectivity of Aeroflex hybrid-compatible PXI modules, the PXI parallel local bus LBL[0]–[12] disappears, to be replaced by the serial connection LBL[6], which is typically used to provide list addresses to a 3010 Series RF Synthesizer.

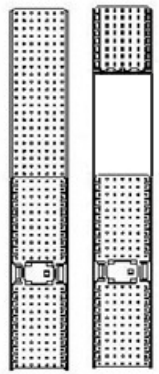


Fig. 1 Standard PXI 1-slot connector (L) and hybrid-compatible PXI connector (R)

This table shows which Aeroflex PXI digital RF signal generator modules fit only in a standard 1-slot, and which fit in both hybrid-compatible and standard slots:

3020A	Standard PXI 1-slot
3020C	Hybrid-compatible and standard PXI 1-slot
3021C	Hybrid-compatible and standard PXI 1-slot
3025	Standard PXI 1-slot
3025C	Hybrid-compatible and standard PXI 1-slot
3026C	Hybrid-compatible and standard PXI 1-slot

GENERAL INFORMATION

Introduction

This is the user manual for the 3020A, 3020C, 3021C, 3025, 3025C and 3026C Digital RF Signal Generators, which are referred to generically in this document as '3020 Series'.

These Digital RF Signal Generators operate over the following frequency ranges:

3020A	250 MHz to 2.7 GHz
3020C	1 MHz to 3 GHz (usable to 100 kHz)
3021C	100 kHz to 3 GHz
3025	100 MHz to 6 GHz (usable to 76 MHz)
3025C	1 MHz to 6 GHz (usable to 100 kHz)
3026C	1 MHz to 6 GHz

and the following peak power level ranges:

	≤30 MHz	≤85 MHz	≤3 GHz	>3 GHz
3020A	n/a	n/a	–120 dBm to +5 dBm	n/a
3020C	–120 dBm to +6 dBm	–120 dBm to +6 dBm	–120 dBm to +6 dBm	n/a
3021C	–121 dBm to +14 dBm	–121 dBm to +14 dBm	–121 dBm to +17 dBm	n/a
3025	n/a	n/a	–120 dBm to +5 dBm	–120 dBm to +0 dBm
3025C	–120 dBm to +6 dBm	–120 dBm to +6 dBm	–120 dBm to +6 dBm	–120 dBm to +1 dBm
3026C	–120 dBm to +14 dBm	–120 dBm to +17 dBm	–120 dBm to +17 dBm	–120 dBm to +17 dBm

RF output can be continuous wave (CW) or modulated. Modulation can be internal analog AM/FM, internal and external digital IQ, or external vector.

Internal digital IQ modulation is supported by a built-in dual-channel arbitrary waveform generator (ARB). This ARB is compatible with waveforms designed or packaged using the ***IQCreator*** ® software application. Differential baseband I and Q outputs from the ARB are available as an option. External digital IQ modulation is supported via an LVDS data interface.

An external synthesizer provides the local oscillator input signal: the 3010 Series RF Synthesizer is recommended. This and the Digital RF Signal Generator together occupy only three slots in a 3U PXI chassis (four slots for 3021C/3026C).

Applications

The 3020 Series is ideal for generating complex modulated waveforms for WLAN, WMAN, cellular communications, digital radio communications test and measurement applications, satellite and terrestrial TV broadcasting and military communications. When a 3020 Series module is used with other Aeroflex PXI RF modules, complete RF test systems can be implemented easily. High RF accuracy, stability and repeatability ensure consistent measurement results, helping to improve manufacturing yield.

PXI Express compatibility

Those 3020 Series modules which are hybrid slot-compatible PXI-1 peripheral modules (see table) comply fully with the PXI-1 specification, except that the (upper) J2HM connector is replaced by a smaller eHM (XJ4) connector. They are compatible with both standard and PXI Express chassis.

Wide frequency coverage

The frequency range of the 3020 Series makes it ideal for multi-purpose applications in MF, HF, VHF and UHF radio communications, especially important when testing multi-mode cellular terminals.

Low noise and frequency-agile

When used with a 3010 Series synthesizer, the 3020 Series provides the low noise and high switching speed necessary for high-productivity RFIC testing or the stimulus to frequency-hopping radios.

RF level accuracy and bursting

The 3020 Series maintains accurate RF output levels to typically ±0.3 dB, and can generate modulated RF bursts to simulate TDMA signal characteristics.

IQ digital modulation

The 3020 Series provides high-quality digital modulation suitable for all common radio communications applications, either from the internal ARB or from an external source via the LVDS data connector.

Analog I &Q inputs and outputs (optional)

The 3020 Series can provide baseband I and Q output and CW RF output simultaneously. Differential analog I and Q outputs from the ARB are provided, with control of differential output level, DC bias and offset voltage.

IQ vector modulation

Analog I and Q inputs can be used to generate wideband vector modulation from external analog I and Q sources such as test instruments and device outputs.

Arbitrary waveform generator (ARB)

The ARB can store 128 Msamples (or 0.5 Gsamples with Option 04 fitted) in 3020C/3021C/3025C/3026C, or 32 Msamples in 3020A/3025, either as a single long waveform or any number of smaller waveforms up to the capacity limit of the sample memory. Waveforms transfer quickly between the PXI controller and the ARB because of the wide bandwidth of the PCI backplane. Playback times of more than 30 minutes are possible, longer if ARB sequencing is used.

ARB sequencing

ARB sequencing provides a method for extending the effective ARB sample memory as well as providing a flexible way to compile test sequences. You can define up to 128 sequence steps, each of which defines an ARB file from a selection of up to 1 million (128 when in List mode) (3020C/3021C/3025C/3026C), or up to 64 (3020A/3025), and play it a chosen number of times before continuing on to the next file in the ARB sequence.

Triggering and synchronization

The 3020 Series provides flexible, configurable triggering facilities from inputs on the front panel or the PXI backplane. Triggers can be used for addressed selection or stepped incrementing of list mode. Triggers can generate power bursts and can be programmed into ARB waveforms to provide trigger outputs for other instruments.

A configurable routing matrix provides flexibility as to how you interconnect signals on the PXI backplane, the LVDS and TTL front-panel inputs, and the module's internal functions. Predefined routing scenarios can be loaded, or new scenarios created to meet particular requirements.

List mode

List mode enables very fast settling times for new signal configurations. In list mode, up to 128 internal hardware settings are pre-calculated and stored, providing fast switching of frequency and level whilst maintaining RF output accuracy. List addresses are sourced externally or from an internal counter driven by the test application controlling the 3020 Series module.

Software

A 3020 Series module is supplied with a VXI PNP driver and soft front panel for use as a standalone module. It is also supplied with an instrument-level signal generator soft front panel, a dll and a COM object, for use with a 3010 Series RF synthesizer.

Refer to the guide *Getting Started with afSigGen* (part no. 46892/678), available on the PXI Modules CD-ROM part no. 46886/028.

IQCreator ® allows you to design your own, or system-specific, complex modulation files for use with a 3020 Series module's internal ARB.

PXI Studio, also supplied with the module, configures your PXI modules as logical instruments using an intuitive and powerful graphical interface. PXI Studio provides comprehensive signal generator, digitizer and spectrum analyzer applications, and optional analysis plug-ins to suit specific communications systems.

RF Investigator, also supplied with the module, is an application that provides combined operation of all Aeroflex 3000 Series modules from a single user interface, especially useful for acceptance testing.

Deliverable items

- 3020 Series RF Signal Generator PXI module
- PXI Modules CD-ROM (part no. 46886/028), containing soft front panels, drivers, application software, data sheets, installation guides, safety instructions, getting started and user manuals for this and other modules in the 3000 Series
- *3000 Series PXI Modules Safety Instructions*: printed item, part no. 46882/882
- SMA connector cable: part no. 43139/738; all modules except 3021C/3026C
- SMA connector cable: part no. 43139/739; 3021C/3026C only

Cleaning

Before commencing any cleaning, switch off the chassis and disconnect it from the supply. You can wipe the front panel of the module using a soft cloth moistened in water, taking care not to wet the connectors. Do not use aerosol or liquid solvent cleaners.

Putting into storage

If you put the module into storage, ensure that the following conditions are not exceeded:

Temperature range:	–20 to +70°C (–4 to +158°F)
Humidity:	5 to 93%, non-condensing

Specifications

For the latest specifications, see the data sheet included on the CD-ROM (part no. 46886/028) or go to the Aeroflex website.

All 3030 Series specifications are defined when used in conjunction with the 3010/11 RF Synthesizer PXI module and driver software supplied with the module.

Calibration and servicing

The recommended calibration interval is 24 months.

There are no user-serviceable parts in these modules; if any attention is needed, return the module to your Aeroflex agent.

INSTALLATION

WARNING

Initial visual inspection

Refer to the *3000 Series Common Installation Guide* part no. 46892/663 on the PXI Modules CD-ROM, part no. 46886/028.

CAUTION

Handling precautions

Refer to the *3000 Series Common Installation Guide* part no. 46892/663 on the PXI Modules CD-ROM, part no. 46886/028.

Hardware installation

Installing the module into the PXI chassis

Refer to the *3000 Series Common Installation Guide* part no. 46892/663 and *Installation Guide for Chassis* part no. 46882/697 on the PXI Modules CD-ROM, part no. 46886/028.

Connector care and maintenance

How to connect and torque an SMA connector

1 First, ensure that the mating halves of the connector are correctly aligned.

2 Next, engage the threads of the nut and tighten it by hand, ensuring that the mating halves do not move relative to each other.

3 Then use a torque spanner to tighten the connector, in order to ensure consistent matching and to avoid mechanical stress.

Torque settings for connectors are:

0.56 Nm test torque (development use, semi-permanent installations)

1 Nm final torque (permanent installations)

Never use pliers to tighten connectors.

CAUTION

Overtightening will cause damage!

Maintenance

SMA

Clean connectors regularly, using a cotton bud dipped in isopropyl alcohol. Wipe within the connector cavity, then use a dry cotton bud to finish off. Check for any deposits.

Do not use other cleaners, as they can cause damage to the plastic insulators within the connectors.

Cap unused connectors.

PCI

Protect PCI connector pins by keeping modules in their original packing when not fitted in the rack.

OPERATION

Front-panel connectors

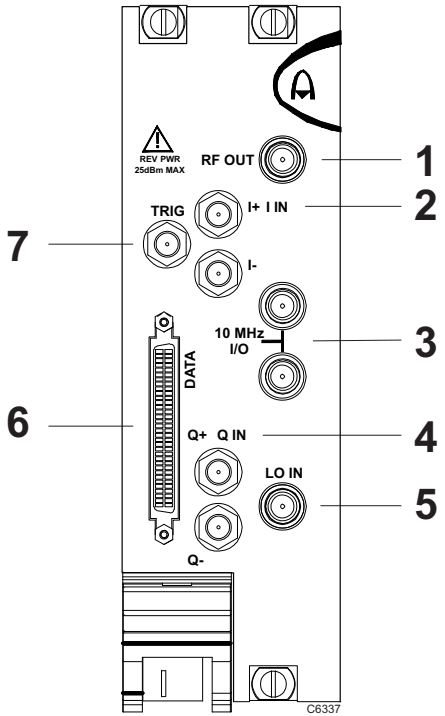


Fig. 2 ***3020A/3020C/3025/3025C*** *front panel*

1	RF OUT	SMA socket, 50 Ω.
2	I+ , I– , I IN Option 01 only	Analog I output (I+ and I–), 50Ω single-ended, 100 Ω differential. SMB sockets. Analog I input (I IN), selectable 50Ω/100 kΩ.
3	10 MHz I/O	Two SMA I/O sockets in parallel. **Input** External frequency standard input for sampling clock. 0.4 to 4 V pk-pk into 50 Ω. **Output** Link-through from input.
4	Q+ , Q– , Q IN Option 01 only.	Analog Q output (Q+ and Q–), 50Ω single-ended, 100 Ω differential. SMB sockets, 50 Ω. Analog Q input (Q IN), selectable 50Ω/100 kΩ.
5	LO IN	1.5 to 3 GHz, nominally 0 dBm. SMA socket, 50 Ω.
6	DATA	68-way VHDCI connector for LVDS data I/O, 14-bit IQ digital data input. See Appendix B for details.
7	TRIG	Input, TTL +ve or –ve edge. SMB socket, 50 Ω.

CAUTION **Maximum safe power**

Reverse power handling: not to exceed **+20 dBm** (3020A), **+25 dBm** (all other models)

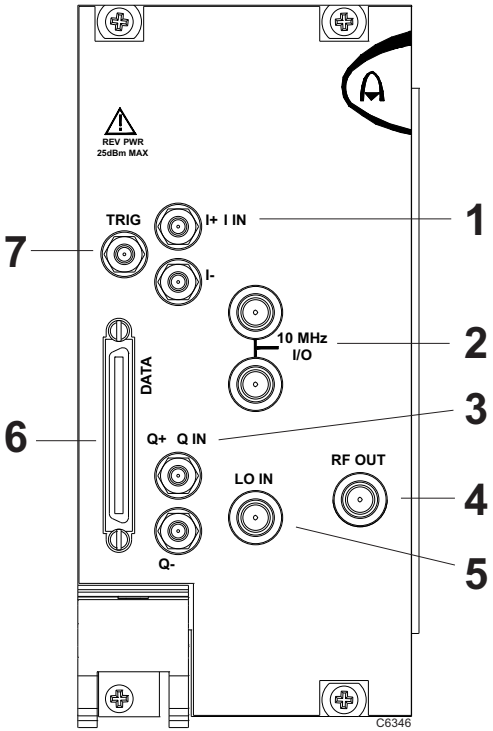


Fig. 3 ***3021C/3026C*** *front panel*

1	I+ , I– , I IN Option 01 only	Analog I output (I+ and I–), 50Ω single-ended, 100 Ω differential. SMB sockets. Analog I input (I IN), selectable 50Ω/100 kΩ.
2	10 MHz I/O	Two SMA I/O sockets in parallel. **Input** External frequency standard input for sampling clock. 0.4 to 4 V pk-pk into 50 Ω. **Output** Link-through from input.
3	Q+ , Q– , Q IN Option 01 only.	Analog Q output (Q+ and Q–), 50Ω single-ended, 100 Ω differential. SMB sockets, 50 Ω. Analog Q input (Q IN), selectable 50Ω/100 kΩ.
4	RF OUT	SMA socket, 50 Ω.
5	LO IN	1.5 to 3 GHz, nominally 0 dBm. SMA socket, 50 Ω.
6	DATA	68-way VHDCI connector for LVDS data I/O, 14-bit IQ digital data input. See Appendix B for details.
7	TRIG	Input, TTL +ve or –ve edge. SMB socket, 50 Ω.

CAUTION **Maximum safe power**

Reverse power handling: not to exceed **+25 dBm**

Soft front panel (af3020_sfp)

The soft front panel provides a graphical interface for operating the module. It is intended for testing and diagnosing, for demonstration and training, and for basic operation of the module. It represents most of the functions available in the instrument driver. It is not however a comprehensive application suitable for measurements; for this, use the afSigGen DLL, the afcomSigGen COM object, the .net assembly (*afSigGenDotNet.dll*) or PXI Studio.

Installation

The soft front panel is installed during the driver installation process (refer to the *3000 Series PXI Modules Common Installation Guide*, part no. 46892/663, on the PXI Modules CD-ROM).

Access the soft front panel from the Windows Start menu under *Programs\Aeroflex\PXI Module Front Panels\AF3020 Soft Front Panel*. Or open the *AF3020_sfp.exe* file, which if you did not change the default location, is located with the VISA software.. The soft front panel, similar to that in Fig. 4, is displayed.

Detailed help information

Soft front panel controls are all available as driver export functions unless noted otherwise, and are documented in the help files. This user manual provides an overview of the facilities that the module provides and summarizes its operation; however, refer to the help files for detailed descriptions of functions, together with their parameter lists and return values.

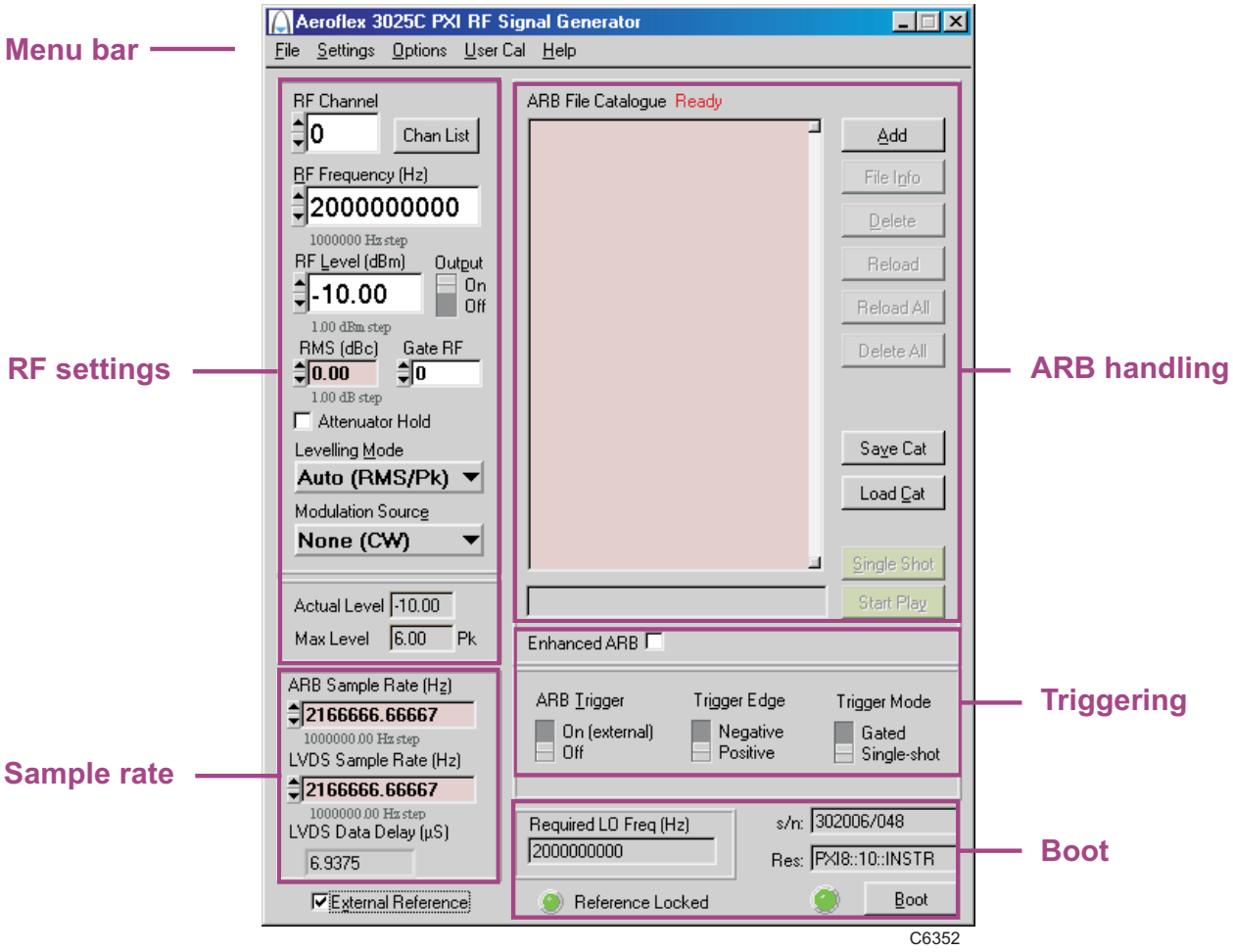


Fig. 4 3025C soft front panel (other 3020 Series panels are similar)

Menu bar

File

Click **File\Exit** on the menu bar to close the application.

Settings

Settings\Load and **Settings\Save** on the menu bar allow you to load and save soft front panel configurations from and to your preferred locations. If you did not change the default location when installing the software, it is the same as for the VISA software (refer to the *3000 Series PXI Modules Common Installation Guide* for details), and configurations are saved as *.ini* files.

> You can edit, copy and paste settings files as required; for example, you may want to save only a new routing setup without changing other parameters. Edit the saved *.ini* file using a text editor (for example, Notepad) to remove unwanted parameters. Ensure only that you do not delete the General (VendorID, DeviceID) and Version (Major/Minor) parameters. Save the changed file. When the settings file is next loaded, the configuration of the soft front panel changes to match the parameters remaining in the settings file, leaving all other settings unchanged.

Settings\Directories on the menu bar lets you choose the locations for your front-panel configuration settings, ARB files and catalogs, synthesizer plugin DLLs and calibration files.

Synthesizer plugins must support a VXI PNP (VISA) RF synthesizer resource capable of 1.5 GHz to 3 GHz. Certain exported functions are also required: refer to online help for details.

Settings\LVDS on the menu bar lets you select the Data Size (14-bit or padded to 16-bit) and Sign (unsigned/signed) to match different data types.

Settings\IQ Bandwidth Correction…: not used on these modules.

Settings\Routing Scenarios on the menu bar allows you to select a predefined routing matrix connection. A tick against the scenario's title shows that it is selected.

If you select a scenario, and then a second, any connected or enabled outputs common to both scenarios are overwritten by the second. Enabled outputs in the first scenario that do not appear in the second also remain active. If the second scenario changes any outputs that were used by the first, the first scenario is invalidated. This process extends to further scenarios.

Settings\Differential IQ on the menu bar appears only when Option 01 'Analog I & Q Inputs and I & Q Outputs' is fitted.

See **Available Options**.

Settings\Analog Modulation on the menu bar displays the screen for setting up internal AM and FM modulation (Fig. 5). Analog modulation is enabled when **Modulation Source** is set to Internal AM or Internal FM.

The modulation source for internal AM/FM analog modulation is a sinusoid with user-settable frequency (modulation rate).

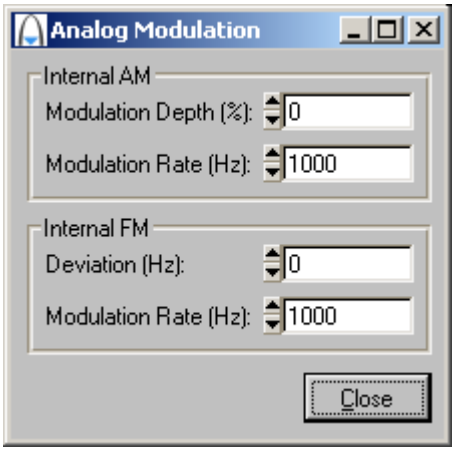


Fig. 5 Analog modulation setup screen

Settings\Routing Matrix on the menu bar displays a matrix that provides interconnection between input and output signals on the PXI backplane bus, the DATA connector, the TRIG connector and the module's internal circuitry, as shown diagrammatically in Fig. 6. This provides great flexibility in how you can route signals between modules.

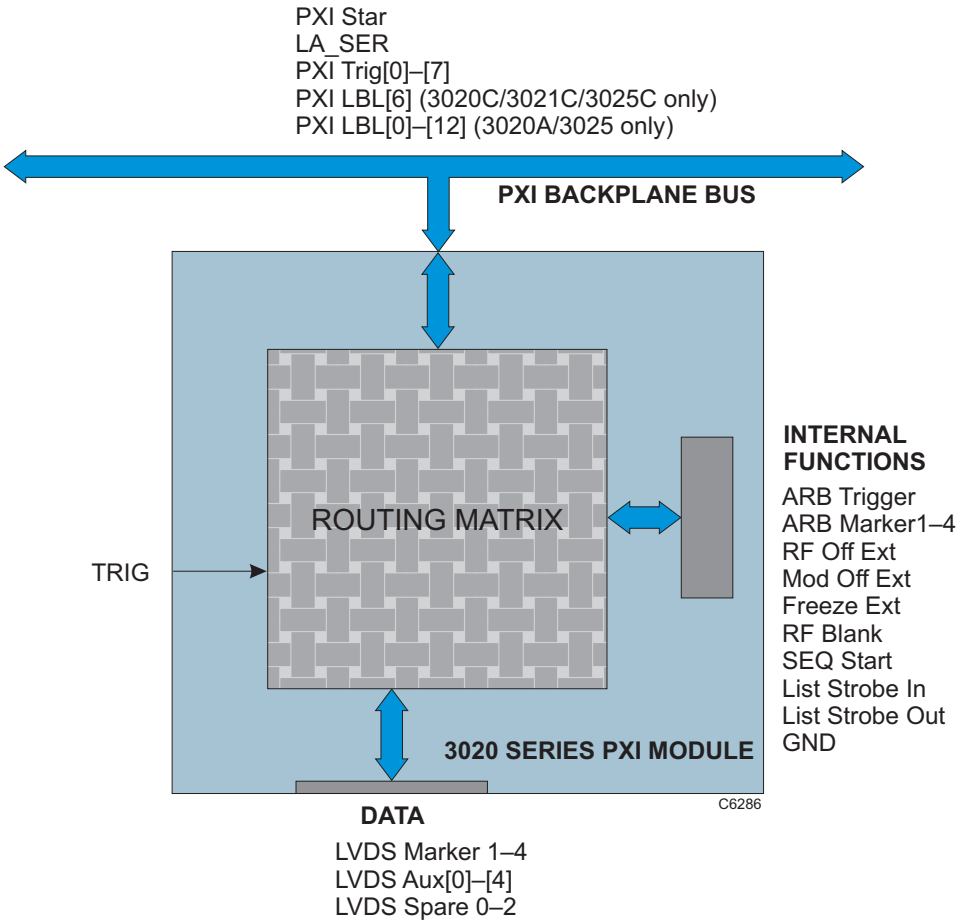


Fig. 6 Routing matrix in 3020 Series

Routing matrix

Use the routing matrix (Fig. 7) to interconnect signals. Output signals form the body of the matrix. Select appropriate input signals from the drop-down menus under each down-arrow to create the interconnections.

Check the boxes to enable the outputs. **Reset** sets all input signals to GND, which is the default state.

When operating the module in default signal generator mode (routing matrix reset), all necessary input, output and trigger signals are available on front-panel DATA, SMA or SMB connectors and there is no need to configure the matrix. If you need to set up particular signal routings, you can define these using the drop-down menus on the matrix and save them using the **Settings\Load** and **Save** commands, or use **Settings\Routing Scenarios** to access pre-set alternative routings, or contact Aeroflex if you need assistance in defining particular routing requirements.

3020 Series are hybrid slot-compatible PXI-1 peripheral modules, and so all but one of the parallel LBL outputs are grayed out and unavailable. Instead, the drop-down menu associated with LBL[6] provides a serial interface LA_SER.

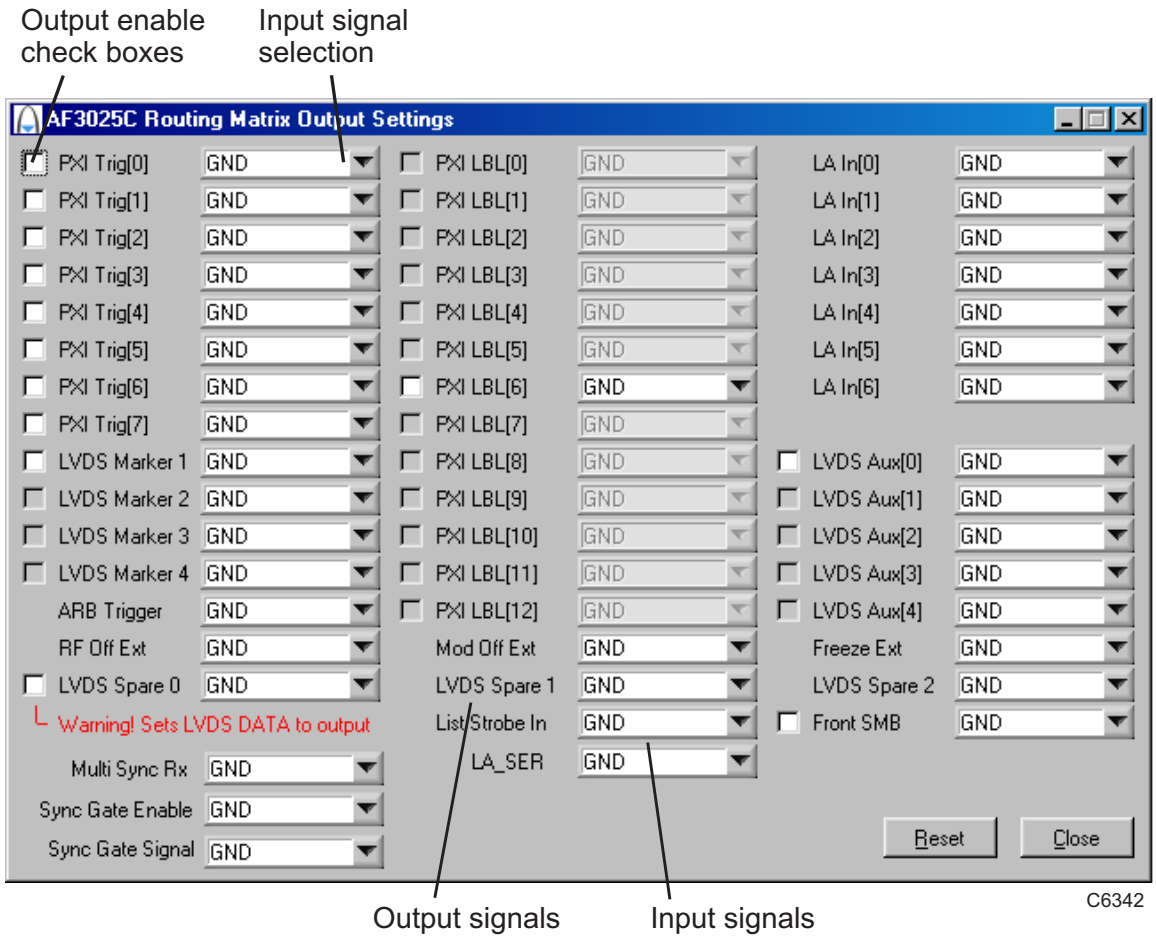


Fig. 7 Routing matrix inputs and outputs (other 3020 Series are similar)

Routing matrix signals are shown in the following tables. All signals are TTL compatible and active high. Note that some signals apply to 3020C/3021C/3025C/3026C or 3020A/3025 only.

***Note**: the labels shown below are prefixed af3020_ROUTE_ when using af3020_32.dll (see af3020_lib_const.h). If using afsiggen (preferred), the labels are prefixed afSigGenDll_rm (see afsiggen help file).*

Routing matrix data destinations: external signals		
Name in SFP	Label	Description
PXI Trig[0]–[7]	PXI_TRIG_N	Eight PXI bus timing and trigger lines (TTL) shared by all modules, which allow one card to co-ordinate the actions of others. Recommended to keep signals below 20 MHz. Each output can be enabled individually.
LVDS Marker 1–4	LVDS_MARKER_N	Four LVDS marker bus lines on the front panel LVDS connector. When enabled, all four bits are outputs.
LVDS Spare 0	LVDS_SPARE_0	Spare LVDS line 0. Note that enabling this output also sets all the LVDS data lines to outputs.
LVDS Spare 1, LVDS Spare 2	LVDS_SPARE_N	Spare LVDS outputs. LVDS_SPARE_1 and LVDS_SPARE_2 are output only.
PXI LBL[0]–[12] *3020A/3025 only*	PXI_LBL_N	13 parallel PXI local bus lines to the adjacent slots on the left of the module. LBL[0]-[7] are typically driven from LA_OUT[0]-[7] to route the list address to an associated 301x module. When using the afsiggen driver in arbseq or hopping mode, the setup of this routing is handled automatically.
PXI LBL[6] *3020C/3021C/3025C/3026C only*	PXI_LBL_6	Only LBL[6] is available on PXI hybrid modules. This is typically used to route the list address to an associated 301x by driving it from the serial list address, LA_SER. When using the afsiggen driver in arbseq or hopping mode, the setup of this routing is handled automatically.
LVDS Aux[0]–[4]	LVDS_AUX_N	Five LVDS auxiliary bus lines. When enabled, all five bits are outputs.
Front SMB	FRONT_SMB	Front panel trigger. Acts as output when enabled.

Routing matrix data destinations: internal signals		
Name in SFP	Label	Description
ARB Trigger	ARB_TRIG	Triggers the internal ARB when in triggered mode.
RF Off Ext	RFOFF_EXT	Blanks the RF output when asserted.
Mod Off Ext	MODOFF_EXT	Disables modulation when asserted.
Freeze Ext	FREEZE_EXT	Freezes the level control loop integrator when asserted.
LA_SER	LA_SER	Selects the list address (serial mode — requires only one control line). To use serial mode via af3020_32.dll, you must set the list address source to EXTERNAL_SERIAL. The SFP does not support this functionality.
LA In[0]–[6]	LA_IN_N	Selects the list address (parallel mode – requires 7 control lines to access all addresses). To use parallel mode via af3020_32.dll, you must set the list address source to EXTERNAL. The SFP does not support this functionality.
List Strobe In	LSTB_IN	List address strobe input (used for parallel mode only)
Sync Gate Signal *3020C/3021C/3025C/3026C only*	TRIG_GATE_SIG	Input signal to the trigger gate.
Sync Gate Enable *3020C/3021C/3025C/3026C only*	TRIG_GATE_EN	Enable signal to the trigger gate. When TRIG_GATE_EN is low, it prevents the TRIG_GATE_SIG signal reaching TRIG_GATE_OUT (see internal data sources). When TRIG_GATE_EN is high, trigger pulses are passed on to TRIG_GATE_OUT.
Multi Sync Rx *3020C/3021C/3025C/3026C only*	MULTI_SYNC_RX	For factory use only.

Routing matrix data sources: external signals

Note that, in general, bidirectional external signals that have been enabled as outputs can still be used as a data source.

Name in SFP	Label	Description
PXI Trig[0]–[7]	PXI_TRIG_N	Signals from the PXI Trigger bus.
PXI Star	PXI_STAR	Dedicated trigger line from the module in slot 2. Input only. Can be used to trigger multiple modules independently with low timing skew.
PXI LBL[0]–[12] *3020A/3025 only*	PXI_LBL_N	13 parallel PXI local bus lines from the adjacent slot on the left of the module. Generally used to drive the list address *to* 301x and not commonly used as a data source.
PXI LBL[6] *3020C/3021C/3025C/3026C only*	PXI_LBL_6	Only LBL[6] is available on PXI hybrid modules.
LVDS Marker 1–4	LVDS_MARKER_N	Four marker bits from the front panel LVDS connector.
LVDS Aux[0]–[4]	LVDS_AUX_N	Five aux bits from the front panel LVDS connector.
LVDS Spare 0	LVDS_SPARE_0	Single spare bit from the front panel LVDS connector.
Front SMB	FRONT_SMB	Data from front panel trigger connector.

Routing matrix data sources: internal signals		
Name in SFP	Label	Description
ARB Marker 1–4	ARB_MARKER_N	Four marker bits from the ARB. Each sample in the .AIQ file has four associated marker bits, which are generated synchronously with the samples.
LA Out[0]–[7]	LA_OUT_N	The currently selected list address in parallel form. These signals are typically routed via PXI_LBL_N to an associated 301x to command it to the same list address.
LSTB Out	LSTB_OUT	Strobe pulse for list address LA_OUT_N. Typically routed via PXI_LBL_N to the associated 301x.
LA_SER	LA_SER	Serial form of LA_OUT list address. This can be used to reduce the number of pins required to communicate the list address. It is generally used on hybrid modules to send the list address to the associated 301x via PXI_LBL_6.
Seq Start	SEQ_START	Indicates the start of the list sequence.
RF Blank	RF_BLANK	Indicates that the RF hardware is changing settings.
SW Trig	SW_TRIG	Software-generated trigger pulse. See af3020_listSoftwareTrigger in the help file.
GND	GND	Logic low
Trig Gate Out *3020C/3021C/3025C/3026C only*	TRIG_GATE_OUT	Output signal from the trigger gate. When SYNC_GATE_EN is high, trigger pulses are passed on to TRIG_GATE_OUT.
Multi Sync Tx *3020C/3021C/3025C/3026C only*	MULTI_SYNC_TX	For factory use only.

Example of using the routing matrix

Configuring the front-panel SMB as a gating signal between PXI Trigger Bus 0 and the ARB trigger:

- Connect Sync Gate Signal to PXI Trig[0]
- Connect ARB Trigger to Sync Gate Out
- Connect Sync Gate Enable to Front SMB.

Analog Modulation

Modulation Depth (%) sets AM modulation depth, in %.

Modulation Rate (Hz) sets AM modulation rate, in Hz.

Deviation (Hz) sets FM deviation, in Hz.

Modulation Rate (Hz) sets FM modulation rate, in Hz.

Settings\DDS on the menu bar (3020C/3021C/3025C only) selects the clock mode for the DDS (direct digital synthesizer). The DDS provides lower frequency (up to 85 MHz) RF signals. For most applications, the clock mode is set to Low Noise (default), which uses the clock provided by the rack's 3010 Series synthesizer module to provide the best noise and spurious performance from the DDS. However, when frequencies are switching rapidly and crossing the 85 MHz threshold (for example, in list mode), delays can occur due to hardware switching. In this case, set the clock mode to Fast, to use the 3020C/3021C/3025C module's own internal clock oscillator and ensure that the signal settling time is as specified on the data sheet.

***Note**: you need **Option 02** ('High speed frequency switching below 85 MHz') fitted to achieve the fastest settling time: refer to the data sheet.*

Options

Click **Options\Edit** on the menu bar to display the options screen (Fig. 8). You may enable or disable additional instrument options if you have the appropriate password (available from the Aeroflex sales desk).

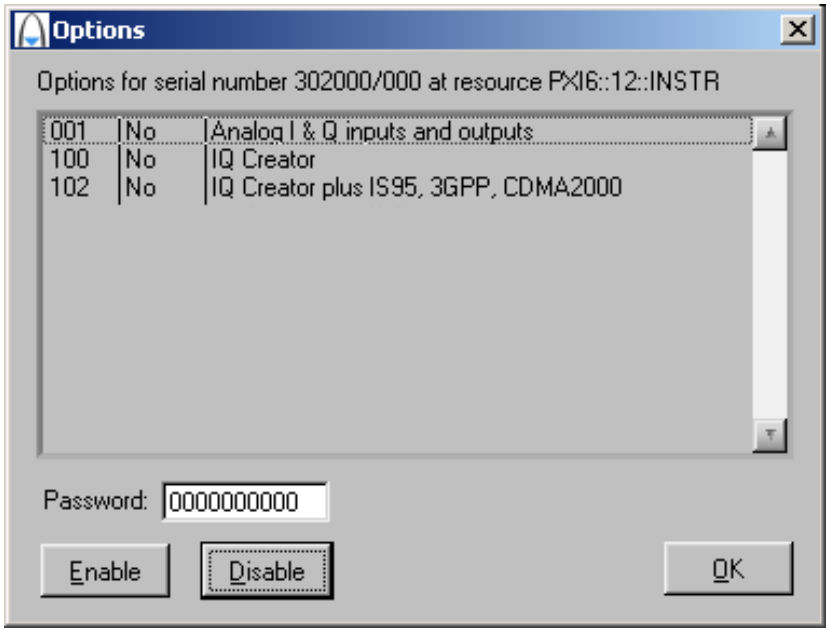


Fig. 8 Options screen (example)

Disabled options are shown grayed out. To enable an option, enter the appropriate password. Click **Enable**. The enabled option is shown highlighted in green. Click **OK**.

User Cal

Click **User Cal** on the menu bar. Calibration is needed to ensure that some specifications — such as carrier leak — are met, and are guaranteed only if a user calibration has been performed. The module calibrates at the current frequency, or at a range of frequencies, and stores the results so that if you change frequency and return again, the calibration still applies.

In some cases, an LO signal is required; the user calibration screen prompts for the LO Plugin Filename. You can browse for this and boot the selected device from the User Calibration screen. The plugin is needed to provide control of the LO when calibrating over a range of frequencies. Two plugins are provided on the PXI modules CD-ROM, and are installed automatically to your chosen location during driver installation. The supplied plugin for use with a 3010 Series module is *af3010_plugin.dll*.

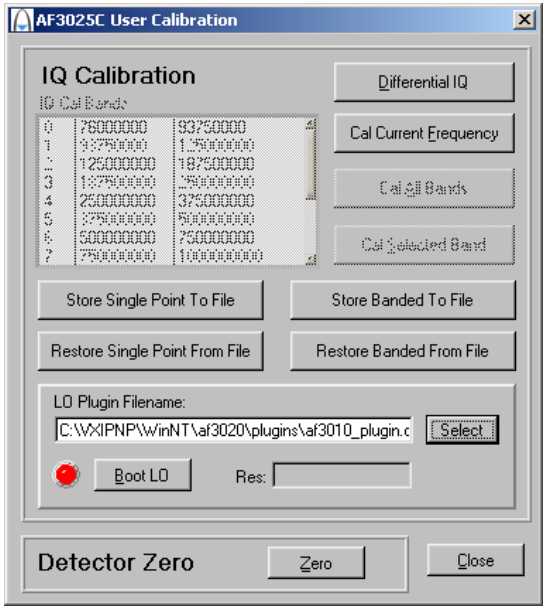


Fig. 9 User calibration screen (other 3020 Series are similar)

IQ Calibration

Differential IQ: there are two differential IQ calibrations:

Cal Outputs is used to null out any DC offset on the differential outputs.

Cal Inputs is used to null out DC offsets on the analog IQ input path. If you apply no signal, this cal nulls DC offsets internal to the module's analog IQ input path. If you apply a nominal 0 V signal level, this cal nulls both user DC offsets and internal module DC offsets.

See also **Differential IQ**.

Cal Current Frequency calibrates the IQ modulator at the current frequency. Calibration is valid for frequencies within ±1 MHz of the current frequency. The plugin is not used, but the LO signal must be present at the correct frequency.

Cal All Bands calibrates the IQ modulator over the entire frequency range of the module and returns the instrument to its current state. The plugin is required.

Cal Selected Band calibrates the IQ modulator over individual bands and returns the instrument to its current state. The plugin is required.

Store Single Point/Banded to File lets you save calibrations using the standard Windows browser. Calibrations are saved as *.ciq* files.

Restore Single Point/Banded from File lets you restore *.ciq* calibrations using the standard Windows browser.

Detector Zero

Zero sets the leveling detector to zero. This ensures that the module meets the level accuracy specified in the data sheet. No LO plugin or LO signal is needed.

Help

Help\Instrument Information on the menu bar provides the module's PXI resource code and serial number, revision numbers for driver, FPGA and PCI, and its last calibration date.

Help\About on the menu bar provides the version and date of the soft front panel.

Boot

Click **Boot** (here) to initialize the module and view the Boot Resource window. Resources available for initializing are shown in blue.

Select the 3020 Series module you want to boot.

Boot default FPGA configuration box.
Check this. Do not change the configuration unless you are advised otherwise.

EEPROM caching box.
Check this, so that when you boot a particular module for the first time, calibration data is read from the module and placed in the local cache that you define in the EEPROM Cache Path. This initial boot time is of the order of 45 seconds. Then check the EEPROM caching box at subsequent power-ups of this module to provide considerably faster boot times. The EEPROM caching box is cleared at each power-down.

Click **OK**. While you select the boot resource, the indicator is amber. Once the module has initialized, the indicator changes to green in a few seconds.

If no calibration data is available, the driver returns a caution. If this happens, return the module for calibration.

s/n:

After the module initializes, this field displays its serial number.

Res:

After the module initializes, this field displays its VISA resource string.

Required LO Freq (Hz)

Shows the frequency that needs to be set on the 3010 Series synthesizer to give the chosen RF frequency at the 3020 Series module's output. Double-click in this field, copy the value, and paste into the RF Frequency (Hz) field on the 3010 Series module's soft front panel.

Reference Locked

This indicator is lit when the 3020 Series module is locked to an external 10 MHz reference signal. If it is not lit, the external reference is missing.

RF settings

The controls available in this group (here) allow you to configure up to 128 channels for frequency, level, leveling mode, and other parameters. These parameters are stored, and are recalled as each channel is selected. This selection can be manual (by clicking the up/down arrows of the RF Channel field) or by list mode operation.

RF Channel

Sets the currently active channel in a range of 0 to 63 (3020A/3025) or 0 to 127 (3020C/3021C/3025C/3026C).

Chan List

Click this to set up each of up to 64 channels (3020A/3025) or 128 channels (3020C/3021C/3025C/3026C). You can edit, copy and paste the settings to simplify setup.

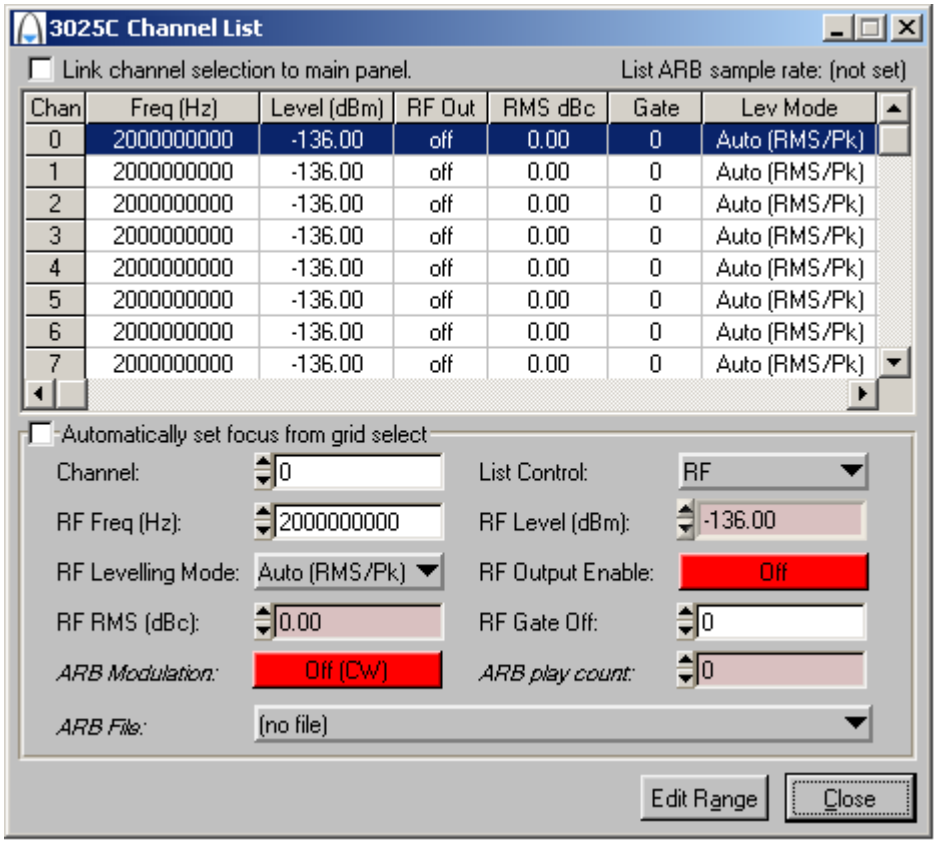


Fig. 10 Edit channel list settings (other 3020 Series are similar)

Edit the grid in the upper part of the screen by means of the fields in the lower part. Edit each channel individually or by range for:

Channel
RF Freq (Hz)
RF Levelling Mode
RF RMS (dBc)
RF Level (dBm)
RF Output Enable
RF Gate Off
ARB Modulation
ARB Play Count
ARB File

Click on the link for details.

Check the **Automatically set focus from grid select** box to make the associated field active when you click on a channel parameter in the grid.

If you check the **Link channel selection to main panel** box, changing the channel on this screen also changes the active channel (as shown on the soft front panel) and vice versa.

Click **Edit Range** to display the Edit Channel Range screen (Fig. 11), which lets you apply changes to a set of channels simultaneously, speeding up channel setup.

Define start and finish values for address numbers in the **Chan range, from:** and **to:** fields.

Insert values and click **Set** for each field. You are asked to confirm each action. When finished, click **Close** to return to the Channel List screen.

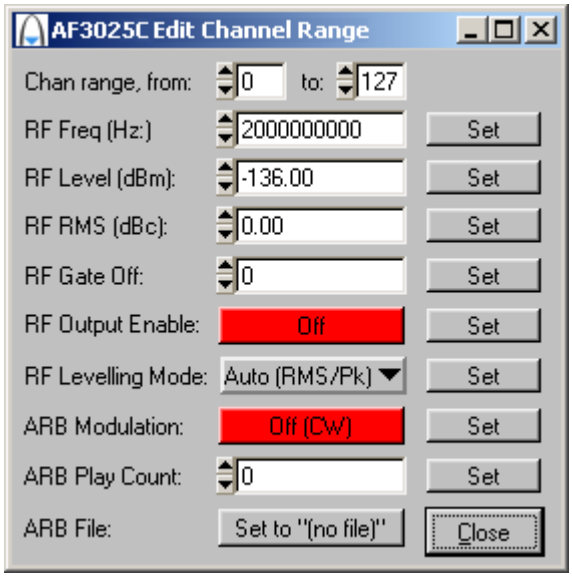


Fig. 11 Edit all channel settings (other 3020 Series are similar)

RF Frequency (Hz)

Set the output frequency using the up/down arrows or by entering the frequency in Hz or scientific (e) notation.

***Note**: the* Required LO Freq (Hz*) box shows the frequency that needs to be set on the 3010 Series synthesizer to give the chosen RF frequency at the 3020 Series module's output.*

Step size: double-click on the step value under the frequency field to set up the size of frequency step.

RF Level (dBm)

Set the output level using the up/down arrows or by entering the value in dBm.

Step size: double-click on the step value under the RF level field to set up the size of level step.

Output

On/Off: enable or disable the RF output.

RMS (dBc)

IQCreator ® files contain header information that indicates the RMS power level of the waveform. When using other sources of IQ, this information may not be present, in which case the RMS value needs to be entered in order to achieve the calibrated output level.

For files that do not contain RMS level header information, you can enter the RMS value of the signal here, and select **RMS** in the Levelling Mode field. The power output then matches that selected in the RF Level (dBm) field.

Gate RF

If set to 1 (enabled), this turns the RF output for the active channel off when $\sqrt{(I^2 + Q^2)}$ is near to zero. This minimizes IQ leakage to a nominal –80 dBc during periods when the signal is 'off'.

ARB Modulation

Sets ARB modulation off or on. Effective only when List Control is set to RF & ARB. When set to Off (CW), the output becomes CW at the level specified.

ARB Play Count

Sets the number of ARB cycles to play, from 0 to 4095. 0 represents continuous play. Effective only when List Control is set to RF & ARB.

ARB File

Displays the standard file name in *.aiq* format. The file must already be loaded in the ARB File Catalogue.

The first ARB file you select for entry defines the sample rate (shown top right in the Channel List screen). Any other ARB file selected must have the same sample rate.

The software automatically fills all succeeding channels in the list with the last-entered ARB file. These 'filler' files are shown with a +--> prefix to distinguish them from the file that you entered.

Attenuator Hold

As the step attenuator changes range, small changes in VSWR can occur. Check the box to freeze the attenuator on its current range.

The maximum positive excursion is restricted to the 6 dB range of the attenuator pad (8 dB, 3020A only), but you can reduce the RF level over a range of up to 40 dB. However, the level accuracy specification is invalid if you exceed the pad's range by more than −3 dB (for CW). This figure reduces for modulated waveforms.

Attenuator hold is intended to remove pad switching effects when you are making measurements close to the switching point. Unlike conventional signal generators, it does not attempt to maintain level accuracy over a wide range.

With **attenuator hold disabled**, the RF level hardware is set for optimum level accuracy and spectral purity, and changes to the attenuator setting are possible.

Note that level accuracy and spectral purity cannot be guaranteed outside the normal level range.

The current active RF channel cannot be changed while attenuator hold is on.

Levelling Mode

Leveling mode	Internal ARB	External Analogue IQ inputs (Opt. 01)
Auto (RMS/Pk)	Sets leveling automatically to RMS for ARB files that contain appropriate header information (***IQCreator***® files). The set level is RMS. If the RMS value is unavailable, or for inputs via the DATA connector, peak mode is selected automatically.	The set level is for $\sqrt{I^2+Q^2}=0.5V$. Headroom is left for the signals to peak at I=Q=0.5 V. Equivalent to using RMS mode with "RMS (dBc)" set to –3 dB.
Frozen	When frozen mode is selected, the leveling integrator is held at its current value and the system operates open-loop. To recalibrate for temperature changes, switch back to one of the other leveling modes, then back to frozen mode. This mode is advantageous for certain pulsed signals that cannot be easily leveled.	As for Auto mode. Note that the leveling system is always open-loop during external analog IQ operation. The leveling mode selects the reference power level. The system recalibrates to the internal reference voltage whenever the leveling mode, frequency or level is changed.
Peak	Causes the set RF Level to appear at the RF output if you apply full-scale I and Q sample values. As I and Q are decreased, the output decreases proportionally.	The set level is for I=Q=0.5 V Note that at no time should I or Q exceed 0.5 V in any mode, or clipping may occur. For example, do not use I=0, Q=0.707 V.
RMS	Causes the set RF Level to appear at the RF output if the RMS value of the applied IQ data stream equals the value set in the RMS (dBc) field. When you select this leveling mode, the RMS (dBc) field is set to a default value of 0. Note that the values are with respect to I=Q=Max.	You can enter the RMS level of your signal with respect to I=Q=0.5 V. The set level is then in RMS. For example if your signal is $\sqrt{I^2+Q^2}=0.25V$, you would set RMS (dBc) to –9 dB. If you then set -10 dBm, you should get nominally -10 dBm RMS.

***Note**: the maximum power specified on the datasheet is for I=Q=Max (I=Q=0.5 V for analog IQ inputs). This is the same in all modes, and the set level is clipped to avoid exceeding this limit. For example, if the relative RMS level is –3 dBc, the maximum set level in RMS mode is 3 dB below maximum. You are still able to reach the maximum level if you input I=Q=Max.*

Modulation Source

Select between:

LVDS (external modulation via DATA connector on front panel)
ARB (internal modulation using the arbitrary waveform generator)
None (CW) (no modulation, carrier wave only)
Internal AM
Internal FM
External Analog (vector modulation) (allows use of IQ analog inputs when Option 001 is fitted)

Actual Level

Shows the current actual output level achieved by the module. A red indicator beside the RF Level (dBm) field shows either that attenuator hold is enabled or that the output level is not achieving the level requested.

Max Level

Shows the maximum possible output achievable by the module for the current settings and waveform selected.

Sample rate

These controls are here.

ARB Sample Rate (Hz)

Set the ARB's sample rate when Modulation Source is set to ARB. This is necessary only when the ARB file contains no header (files not generated using ***IQCreator*** ®).

LVDS Sample Rate (Hz)

Sets the LVDS sample rate when Modulation Source is set to LVDS. The instrument interpolates the frequency up to 66 MHz (3020A/3025) or 90 MHz (3020C/3021C/3025C/3026C).

External Reference

Checked:	External 10 MHz reference via front-panel SMA connector
Unchecked:	10 MHz reference from PXI backplane.

ARB handling

These controls are here.

Introduction

The ARB is a dual-channel arbitrary waveform IQ baseband source generator. It is used to generate signals from samples stored in non-volatile memory. Four marker bits may be stored with the samples, and these are processed to maintain their time relationship to the output waveforms.

IQCreator ® is a software package that allows you to create and package an arbitrary waveform file that can be loaded onto any 3020 Series digital RF signal generator. It is also possible to package and download files that have been created using other tools. Arbitrary waveforms that can be created by ***IQCreator*** ® cover a wide range of digital modulation schemes.

IQCreator ® is supplied on a CD-ROM together with a *Getting Started* manual (part no. 46892/599) that explains how to create, download and package waveforms to run on the ARB, and a *User Guide* (part no. 46892/627) that details the different modulation schemes supported. ***IQCreator*** ® and its associated documentation are also available to download from the Aeroflex website http://www.aeroflex.com/iqcreator.

ARB File Catalogue

This field displays files currently loaded into the ARB's memory.

Add

Lets you add an ARB waveform to the ARB File Catalogue, using the standard Windows browser. The file must be in *.aiq* format (as generated by ***IQCreator*** ®). Details of the format of ARB files and headers are given in Format of ARB Files.

File Info

Provides information about the currently selected ARB file, such as file name and maximum output level.

Delete

Deletes the currently selected ARB file from the specified catalog.

Reload

Reloads an ARB file from hard disk to the specified catalog.

Reload All

Reloads all ARB files from hard disk. This may improve performance if the ARB memory has become fragmented.

Delete All

Deletes all ARB files from the specified catalog.

Save Cat

Saves a catalog of the currently loaded files into a new folder. This function is available only on the soft front panel.

Load Cat

Loads a previously saved catalog of files from a named folder.

Start Play

Plays the selected ARB file and displays its filename. This function automatically sets the IQ source to ARB, and the VCO frequency appropriate to the file being played.

Triggering

These controls (here) provide trigger setup for the external ARB trigger. External ARB trigger sources are:

PXI backplane (PXI trigger bus)

LVDS AUXiliary inputs (front-panel DATA connector)

TTL TRIG input on front panel (SMB)

Star trigger (star controller card in Slot 2)

Serial local bus (3020C/3021C/3025C/3026C only)

LBL [1–13] (3020A/3025 only)

Select trigger sources with the routing matrix.

ARB Trigger

On (external)	Dependent on Trigger Edge and Trigger Mode
Off	Internal software triggering (see routing matrix input signals):
	ARB Marker
	List address LA Out
	List strobe LSTB Out
	Seq Start
	RF Blank

Trigger Edge

Selects the positive- or negative-going edge of a pulse to trigger the ARB.

Trigger Mode

Gated — Begins playing the ARB file continuously on receipt of the leading edge of a gate pulse. After the trailing edge of the gate, the ARB file continues playing until its end, then stops.

Single-shot — Plays the ARB file once through.

Enhanced ARB

For 3020C/3021C/3025C/3026C only: tick the box to enable an extended set of triggering options.

Fig. 12 Enhanced ARB enabled

ARB Trigger

Any — ARB triggered by a positive- or negative-going signal.

Negative — ARB triggered by a negative-going signal only.

Positive — ARB triggered by a positive-going signal only.

None — No trigger signal is recognized.

Trigger Mode

Start/Retrig	The first trigger edge starts the ARB waveform, the next trigger edge restarts it immediately.
Start/Stop	The first trigger edge starts the ARB waveform, the next trigger edge stops it.
Start Only	The trigger edge starts the waveform. The module then ignores any further trigger inputs until operation is aborted.
Gate	The trigger signal functions as a gate (high = ON) on the ARB output.

Termination

At End	Stops playing at the end of the ARB file.
Instant	The ARB generator stops immediately.

Play Count

Sets the number of times the waveform repeats. Setting this to 0 causes the ARB to play continuously.

Delay

Sets a delay (in seconds) before the ARB starts to run, following a trigger.

Program files

Program files are installed onto your computer from the CD-ROM.

Find registered com DLLs and ocx components, *.net* assemblies, libraries, source and associated help files in the program installation folder on your computer. This is typically:

C:\Program Files\Aeroflex\PXI

All executable C DLLs are installed in:

C:\WINDOWS\system32

Driver export functions

On-line help and functional documentation for driver export functions are available on the CD-ROM supplied with your module. They are installed onto your computer at the same time as the drivers.

Driver installation folder

Find help and functional documentation in the driver installation folder on your computer. If you did not change the default location, this is typically the same as for the VISA software.

Help

Within the driver installation folder are help files that provide descriptions, parameter lists and return values. Help files are provided in three formats:

af3020.doc	3020 Series function documentation	Text file
af3020.hlp	3020 Series Visual BASIC function reference	Windows Help file format
af3020_C.hlp	3020 Series C language function reference	

We recommend that you use the C or Visual Basic formats, as these are easier to navigate.

The file opens at the Contents page:

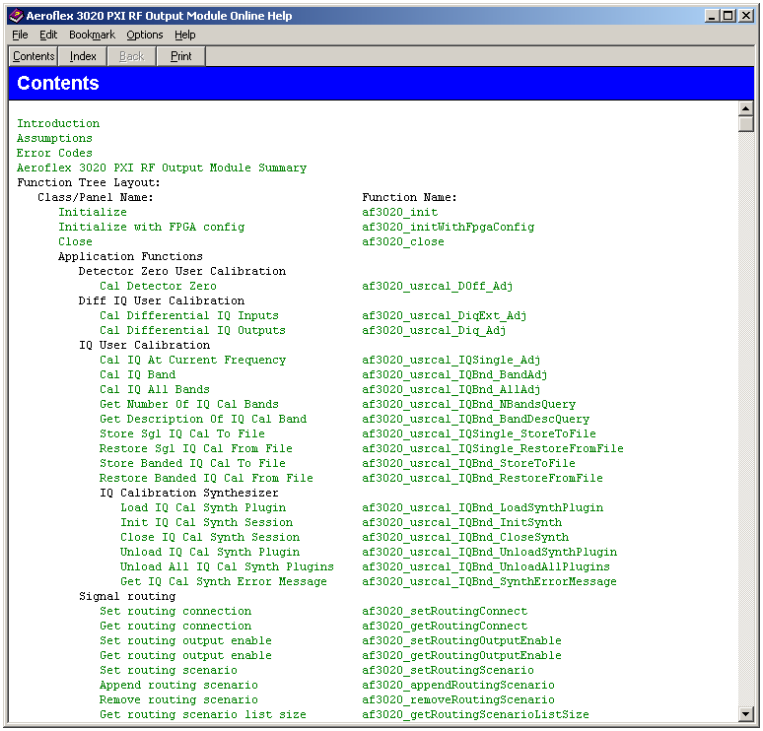


Fig. 13 Online help contents — example

Hyperlinks from here take you to

Introduction

Assumptions

Error codes

Functions listings.

Functions listings

Functions are grouped by type. Click on the hyperlink for details of the function. Each function has a description of its purpose, and may have a list of parameters and return values.

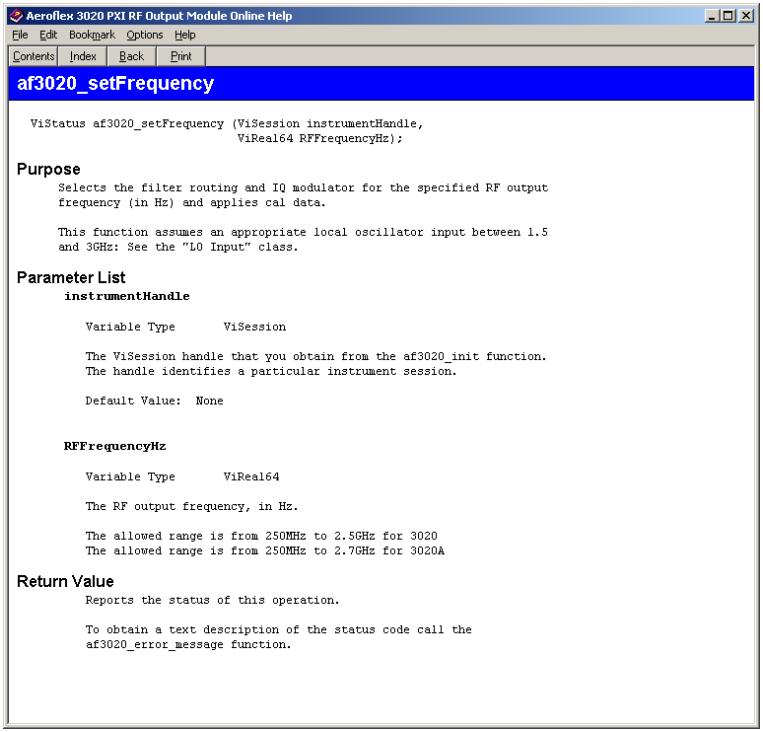


Fig. 14 Function description — example

Available options

Option 01 Analog I & Q inputs and I & Q outputs

Differential IQ

When this option is fitted, **Differential IQ** displays the screen for setting up differential outputs (Fig. 15) and single-ended inputs.

The module provides balanced baseband I and Q **outputs** suitable for feeding devices with differential inputs. Signals that appear on I+ and I–, Q+ and Q–, are of equal magnitude but have opposite polarity. The positive or negative I and Q pairs can also be used as unbalanced single-ended outputs.

The module also accepts single-ended **inputs** into a switchable high or low impedance. Feed analog I signals into I IN, analog Q signals into Q IN.

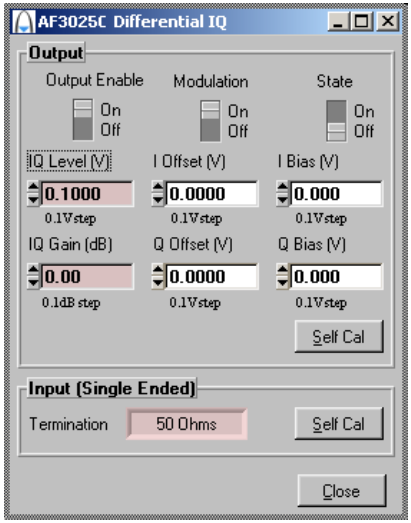


Fig. 15 Differential IQ setup screen

Output Enable enables or disables the differential IQ outputs. When set Off, the output is high impedance. When set On, the output impedance is 50 Ω. **Modulation** enables or disables the bias and offset voltages. When set Off, it zeroes bias, offset and signal voltages.

State enables or disables the ARB signal component. When set Off, it disables the signal but bias and offset levels remain.

IQ Level (V) specifies the peak-peak amplitude of the output signal component (see Fig. 16) into 50 Ω (single-ended) or 100 Ω (differential).

IQ Gain (dB) specifies the relative amplitudes of the I and Q signals. Adding gain (+x dB) to the signal increases the magnitude of the I component by $\frac{x}{2}$dB whilst decreasing the magnitude of the Q component by the same factor. Similarly, removing gain (–x dB) from the signal increases the magnitude of the Q component by $\frac{x}{2}$dB whilst decreasing the magnitude of the I component by the same factor.

I Offset (V) specifies the differential voltage between I+ and I– (see Fig. 16).

Q Offset (V) specifies the differential voltage between Q+ and Q–.

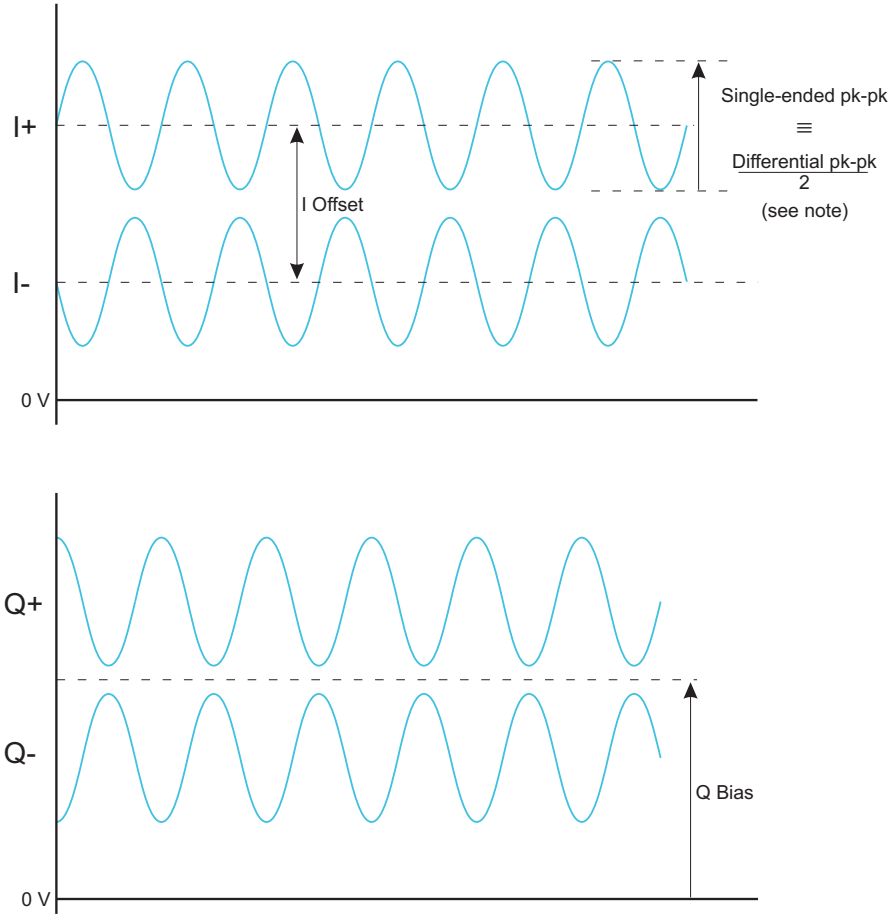
I Bias (V) specifies the common-mode I voltage.

Q Bias (V) specifies the common-mode Q voltage.

Self Cal (output) calibrates the differential IQ by setting input or output levels to 0 V and recalibrating DACs.

Self Cal (input, single-ended) nulls out any DC offset present at the input.

Termination shows the value of input impedance selected. Inputs are enabled when Modulation Source is set to Ext Analog.



Gain
Adding x dB increases I Level by x/2 and decreases Q Level by x/2.
Removing x dB increases Q Level by x/2 and decreases I Level by x/2.

C6169

This diagram represents a condition where the signal is output into a floating 100 Ω load.

***Note**: the differential signal level is twice the single-ended signal level.*

Fig. 16 Differential IQ parameters

Option 02 High speed frequency switching in DDS band

Available on 3020C/3021C/3025C/3026C only.

When this option is fitted, the settling time to within 2 kHz of final frequency is that given in the data sheet. If Option 02 is not fitted, settling time is not faster than 1 ms.

Option 03 1 Gbyte ARB memory

Available on 3020C/3021C/3025C/3026C only.

Allows storage of up to 256 Msamples.

Option 04 2 Gbyte ARB memory

Available on 3020C/3021C/3025C/3026C only.

Allows storage of up to 512 Msamples.

Digital RF signal generator instrument using 3010/3011 and 3020 Series

Refer to *3000 Series PXI Modules Installation Guide for Chassis* (document no. 46892/667), *Getting Started with afSigGen* (document no. 46892/678), and *PXI Studio User Guide* (document no. 46892/809), all supplied on the CD-ROM with the module, for detailed information on creating a fully functional digital signal generator instrument, using a 3020 Series Digital RF Signal Generator module and 3010/3011 RF Synthesizer together. The afSigGen soft front panel and afSigGen dll or afcomSigGen COM object combine the functions of the individual modules to provide a single interface with the appearance and functionality of an integrated instrument.

Appendix A
Format of ARB files

General

The ARB stores digital representations of waveforms. Any number of waveforms can be stored, up to a total capacity of 32 Msamples (3020A/3025) or 128 Msamples (3020C/3021C/3025C/3026C). For 3020C/3021C/3025C/3026C only, this can be extended to 256 or 512 Msamples by fitting Options 3 or 4 respectively. The memory used is volatile.

Each waveform consists of two components, I and Q. When the ARB is enabled and one of the waveforms selected, it is converted into a pair of analog signals that can be used to drive the I and Q channels of the RF modulator, or output as analog baseband IQ when Option 01 is fitted. Waveform data files are created externally and require packaging before they can be used by the ARB.

Each sample contains two 14-bit numbers, one each for I and Q. To minimize the required file size and reduce aliasing problems, the ARB includes an interpolator. The D-A converter runs at a constant 250 M sample/s, and a generic resampler provides any sample rate (including non-integer) up to this value.

A waveform is looped continuously. The rate at which the sample plays is set during file creation and is coded in the header.

***Note**: IQCreator® files with sample rates equal to or less than 66 MHz run on all modules, but files with sample rates greater than 66 MHz run on 3020C/3021C/3025C/3026C only.*

An example showing data rates and sizes for an IS-95 waveform

IS-95 has a chip rate of 1.2288 Mchip/s. For our purposes we will consider a chip to be the significant symbol. Each symbol must be sampled at least four times. This would give a rate of 4.9152 Msample/s. There are 24 576 symbols per 20 ms frame. Four frames would have 98 304 symbols, which after oversampling gives 393 216 samples. As the oversample ratio increases, the file becomes larger.

When the above waveform is selected and played, it is read out of the memory at 4.9152 Msample/s. The ARB interpolates this data stream so that it has a sample rate of 200 Msample/s.

The data is written to the two 16-bit D-A converters. It is resampled to 200 MHz rate before sending to the D-A converters. The analog outputs from the D-A converters are then filtered to remove switching and quantization noise and high-frequency images. The I and Q outputs are then routed to the RF modulator.

Markers

Markers are used to mark important events within the file; for example, the start of a TDMA slot or frame.

Format for header of ARB IQ files (*.aiq)

	Comment	No. of bytes
[File]		
Date=	Date file was created (mm/dd/yyyy)	12
Time=	Time file was created (hh:mm:ss)	10
PackSWVers=nn.nn	SW version of Packager (files that are created using software other than IQCreator® must set nn.nn = 00.00)	5
Samples=	No. of IQ Samples as an ASCII number	8
Title=	Name of AIQ file without extension and without path	80
SampleRate=	In Hz, in steps of 100 Hz, converted from user entry in packager	8
Description=	Description field entered in packager	120
RMS=	RMS value of the stored waveform	9
RelRMS=	RMS relative to maximum (dB)	8
CrestFactor=	Crest factor of stored waveform	8
[Assign]		
Mkr1=	Marker 1 assignment (not used or general)	12
Mkr2=	Marker 2 assignment (not used or general)	12
Mkr3=	Marker 3 assignment (not used or general)	12
Mkr4=	Marker 4 assignment (not used or general)	12

All headers are stored as ASCII strings, each line terminated with CR/LF.

The header is terminated by a ^Z. Data following the header is the IQ and marker data stored as IQIQIQ…

The format is:

bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	S	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	M2	M1

bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	S	I	I	I	I	I	I	I	I	I	I	I	I	I	M4	M3

where Mn = marker number n, S = sign bit.

The last 32-bit value in the file is a checksum that is calculated as the running unsigned sum of the 32-bit numbers.

Appendix B
DATA connector and timing

The DATA connector is a 68-way female VHDCI-type LVDS (low-voltage differential signaling) interface. It can be used to input data and associated control and timing signals.

The DATA connector is shown in Fig. 17. LVDS data conforms to ANSI/TIA/EIA-644.

Fig. 17 DATA connector (looking onto front panel)

The DATA interface provides:

- input for IQ data
- input/output for trigger and marker signals.

The electrical level is LVDS: V_{OH} typically 1.38 V, V_{OL} typically 1.03 V

Table 1 DATA pin-out

Contact	Function	Contact	Function
1	AUX0-	35	AUX0+
2	AUX1–	36	AUX1+
3	AUX2–	37	AUX2+
4	SPARE1–	38	SPARE1+
5	SPARE2–	39	SPARE2+
6	CLK_OUT–	40	CLK_OUT+
7	GND	41	GND
8	CLK_IN–	42	CLK_IN+
9	D0–	43	D0+
10	D1–	44	D1+
11	D2–	45	D2+
12	D3–	46	D3+
13	D4–	47	D4+
14	D5–	48	D5+
15	D6–	49	D6+
16	D7–	50	D7+
17	D8–	51	D8+
18	D9–	52	D9+
19	D10–	53	D10+
20	D11–	54	D11+
21	D12–	55	D12+
22	D13–	56	D13+
23	D14–	57	D14+
24	D15–	58	D15+
25	IQSELECT_IN–	59	I/QSELECT_IN+
26	IQSELECT_OUT–	60	IQSELECT_OUT+
27	SPARE0–	61	SPARE0+

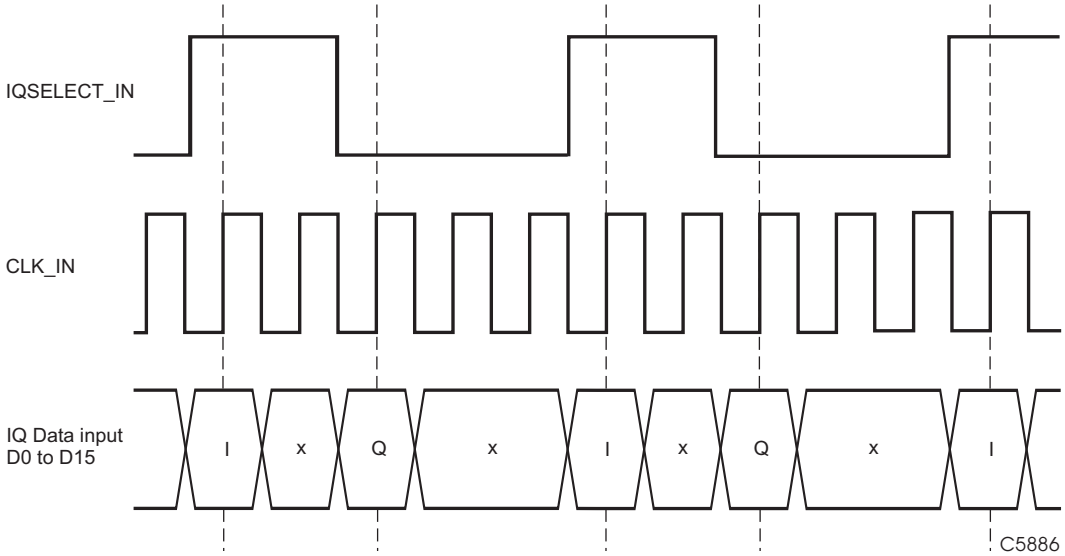
Contact	Function	Contact	Function
28	GND	62	GND
29	MARKER1–	63	MARKER1+
30	MARKER2–	64	MARKER2+
31	MARKER3–	65	MARKER3+
32	MARKER4–	66	MARKER4+
33	AUX3–	67	AUX3+
34	AUX4–	68	AUX4+

LVDS data used as IQ input

Data is supplied to the LVDS interface using a 16-bit bus. The D/A converters are 14 bits and by default the module uses bits [15:2]; however, it is possible to select to use [13:0] instead. Similarly, data is signed two's complement by default, but it is possible to select unsigned instead. See Settings\LVDS.

IQ data pairs are clocked sequentially, with I always followed by Q. I data is clocked into the module on the first CLK_IN edge following IQSELECT_IN going high. Q data is clocked in on the first edge following IQSELECT_IN going low.

Multiple CLK_IN cycles can occur between IQSELECT_IN changing state, and CLK_IN can be any frequency up to 180 MHz. However, the resulting IQ sample pair rate must be the same as the sample rate set for the module. For this to occur, it is important to lock CLK_IN to the same 10 MHz reference that the module is using, otherwise frequency drift will cause periodic data errors.

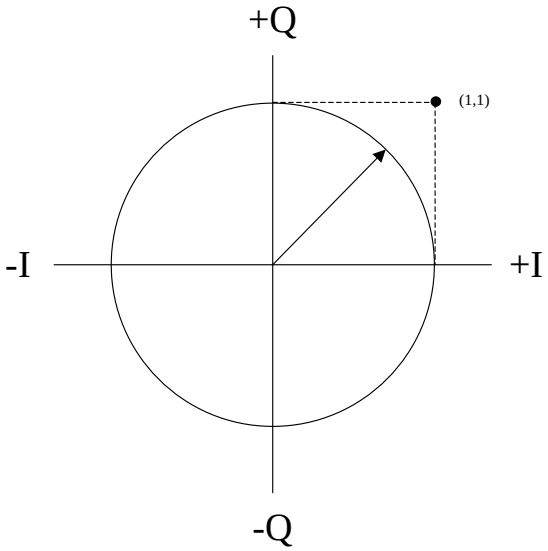


Data in is latched on the rising edge of CLK_IN.

Output power level

The IQ leveling loop is referenced to maximum I and Q level (1,1 on the vector diagram), and the maximum RF power using IQ data is also referenced to this. Output level for a modulated signal with constant envelope (for example, GSM) is reduced by 3 dB on the maximum available CW level. This type of signal will fall on the unit circle.

For complex modulation schemes that include amplitude modulation, the maximum achievable mean power depends on the ratio of mean to peak signal levels. This value is provided in the header information (RelRMS) of files generated in ***IQCreator*** ®.



Markers

There are four marker inputs/outputs on the DATA connector. The markers can be used for triggering and addressing.

BRIEF TECHNICAL DESCRIPTION

Introduction

A 3020 Series module is a PXI digital RF signal generator. It contains IQ modulators, a leveling control system, step attenuators, and a dual-channel arbitrary waveform generator. It is used with an external source, preferably a 3010 Series RF synthesizer, which provides an LO signal. The two modules together then form a digital RF signal generator.

A 3020 Series module comprises three or four printed circuit boards. A logic and control board contains a PCI interface, baseband VCO, IQ ARB, leveling control, direct digital synthesizer (DDS) to generate lower frequency RF signals, and an external LVDS data interface. An RF board is housed in a full clamshell shield, containing RF dividers, IQ modulators, output amplifier and step attenuator. An analog board contains a bias source for the IQ modulators. additional step attenuation and amplification for DDS signals (3020C/3021C/3025C/3026C only) and (when Option 001 is fitted) differential IQ processing. For 3021C/3026C only, a fourth board provides a power amplifier.

Only the logic board connects to the PXI backplane, so power and control to the RF board is routed through the logic board. Ribbon cables interconnect the logic, RF and analog boards, handling power to the RF board, differential analog IQ, analog leveling signals and various switched control signals.

Fig. 18 to Fig. 22 show block schematics for each module type.

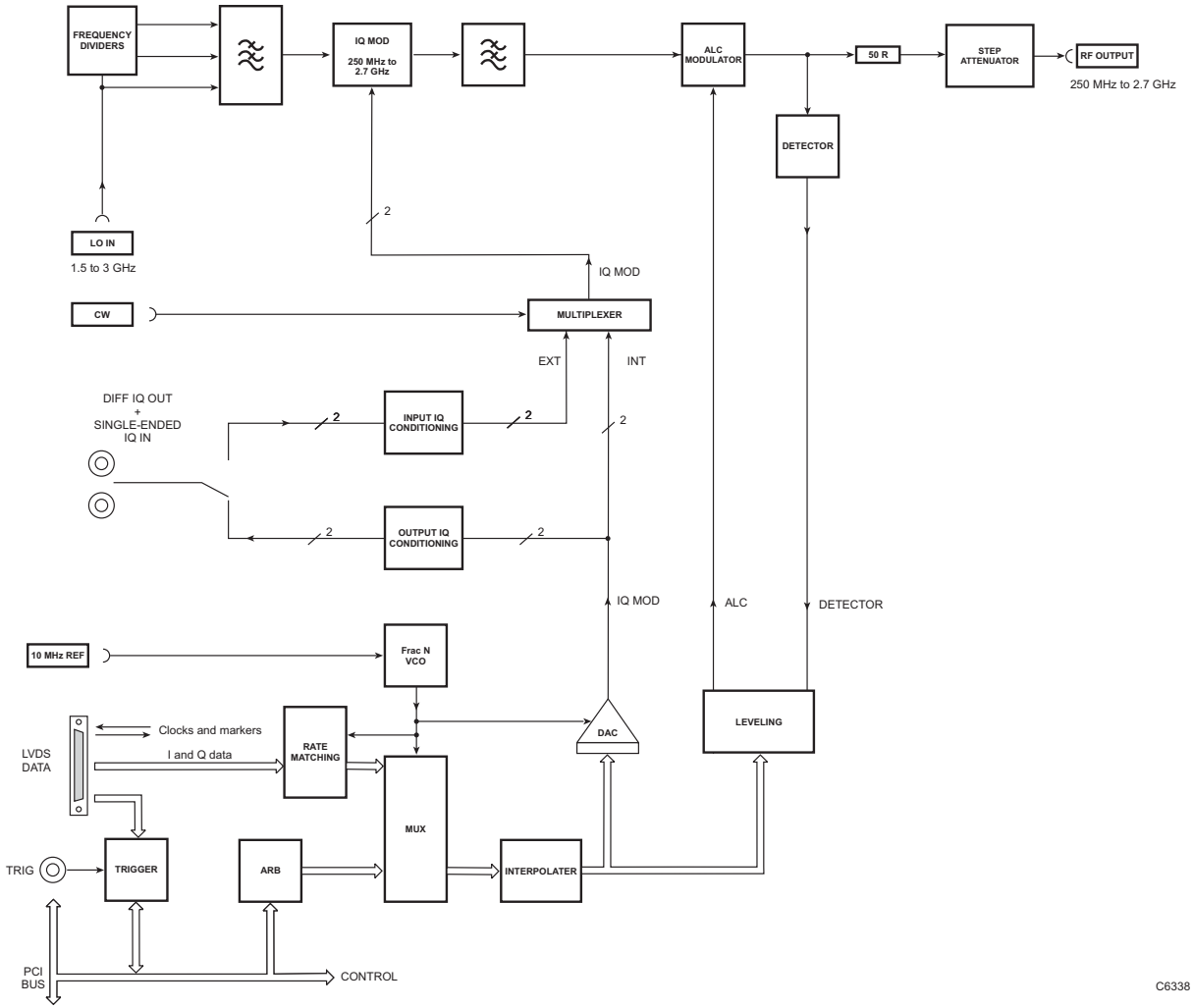


Fig. 18 3020A block schematic diagram

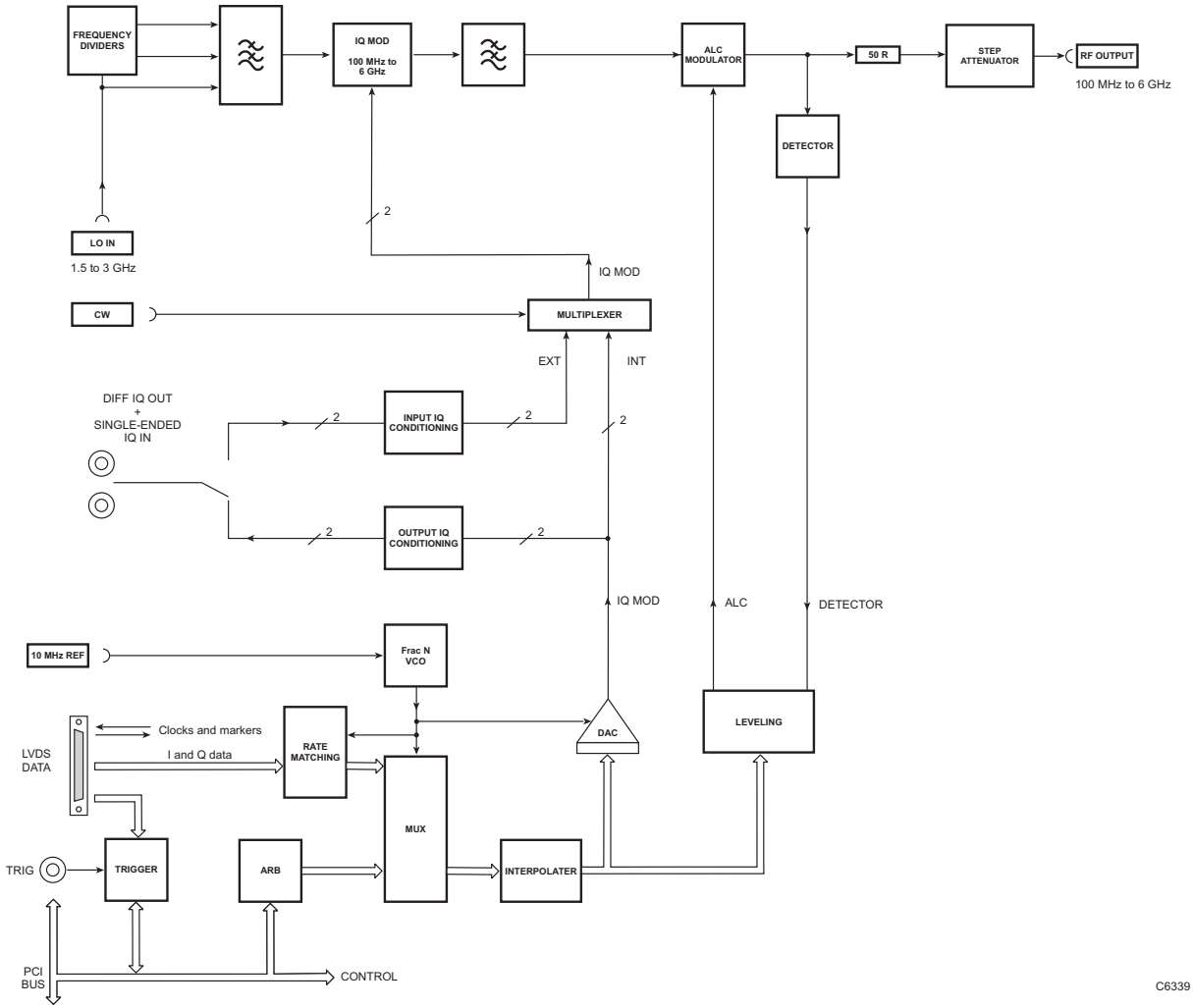


Fig. 19 3025 block schematic diagram

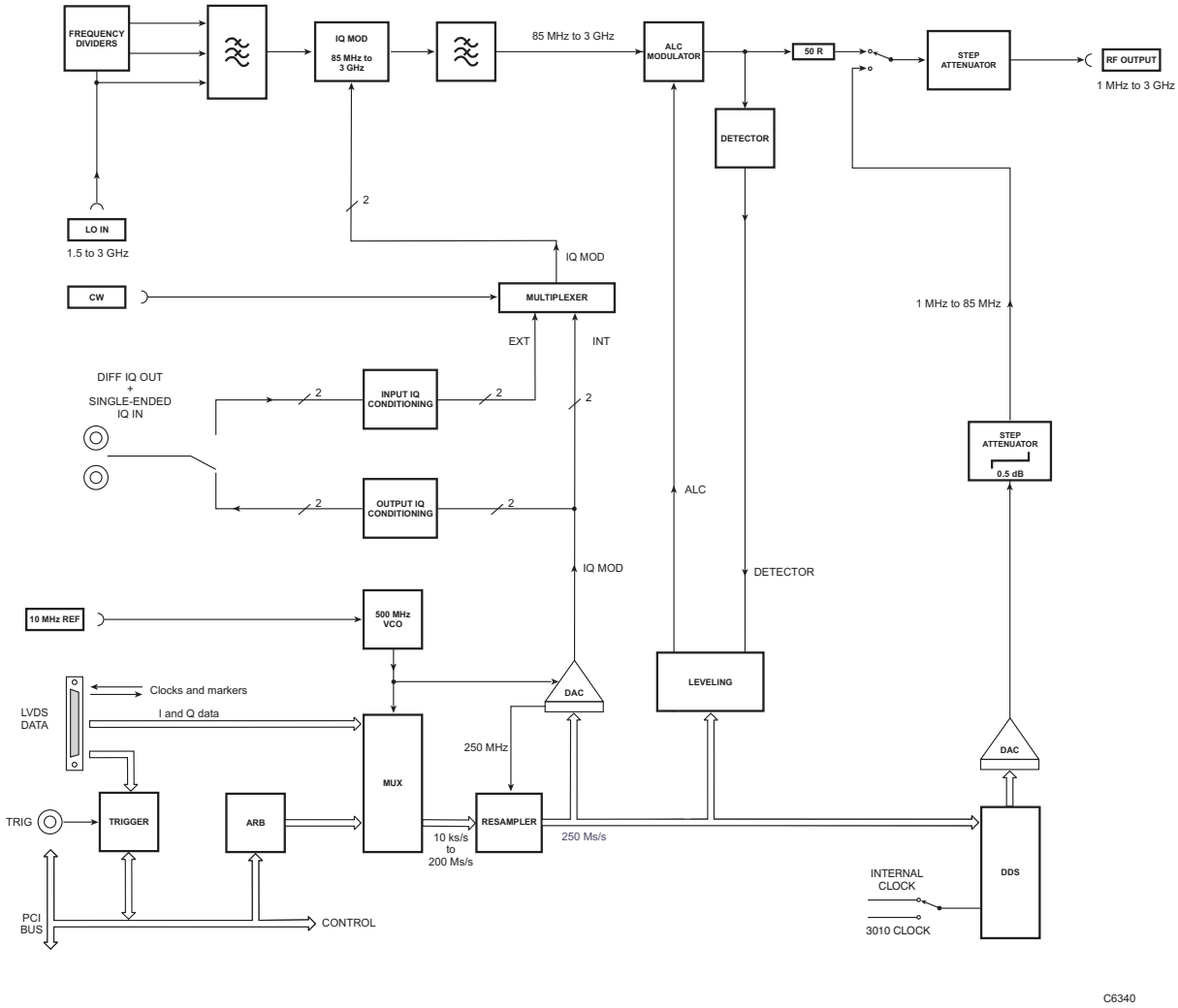


Fig. 20 3020C block schematic diagram

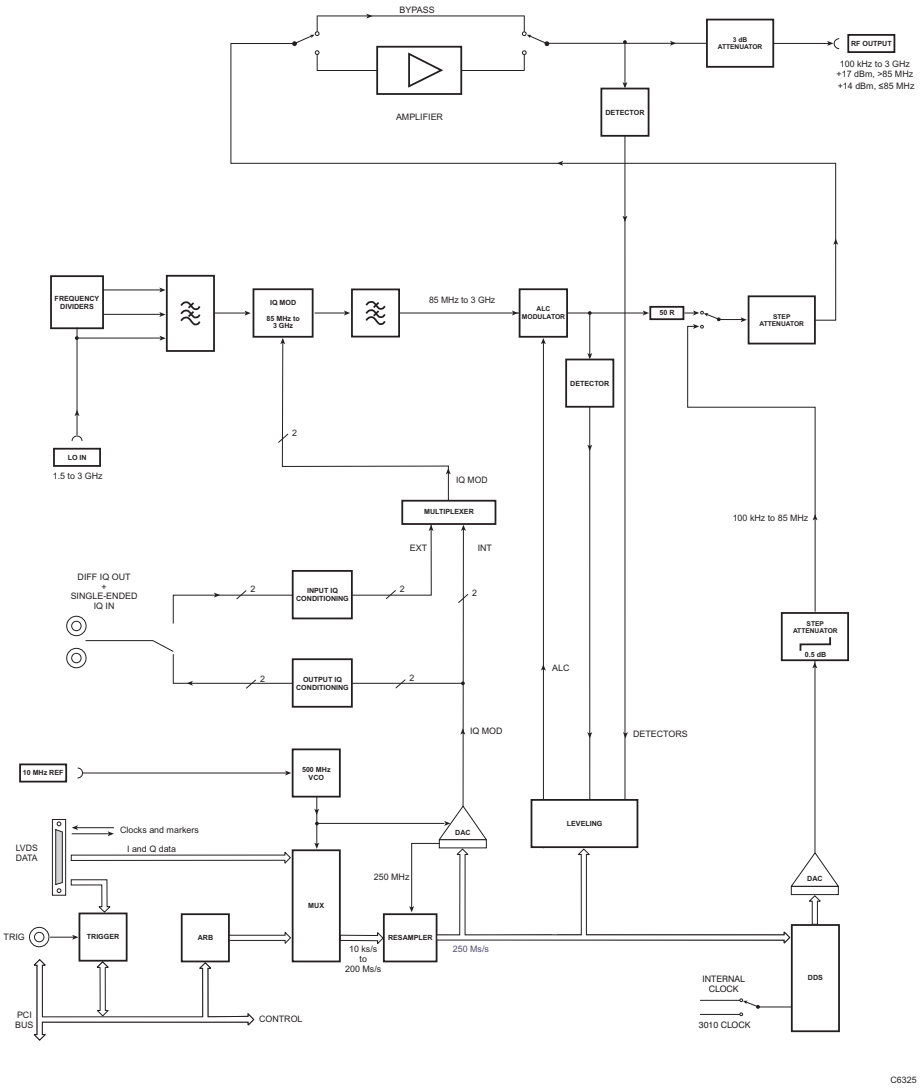


Fig. 21 3021C block schematic diagram

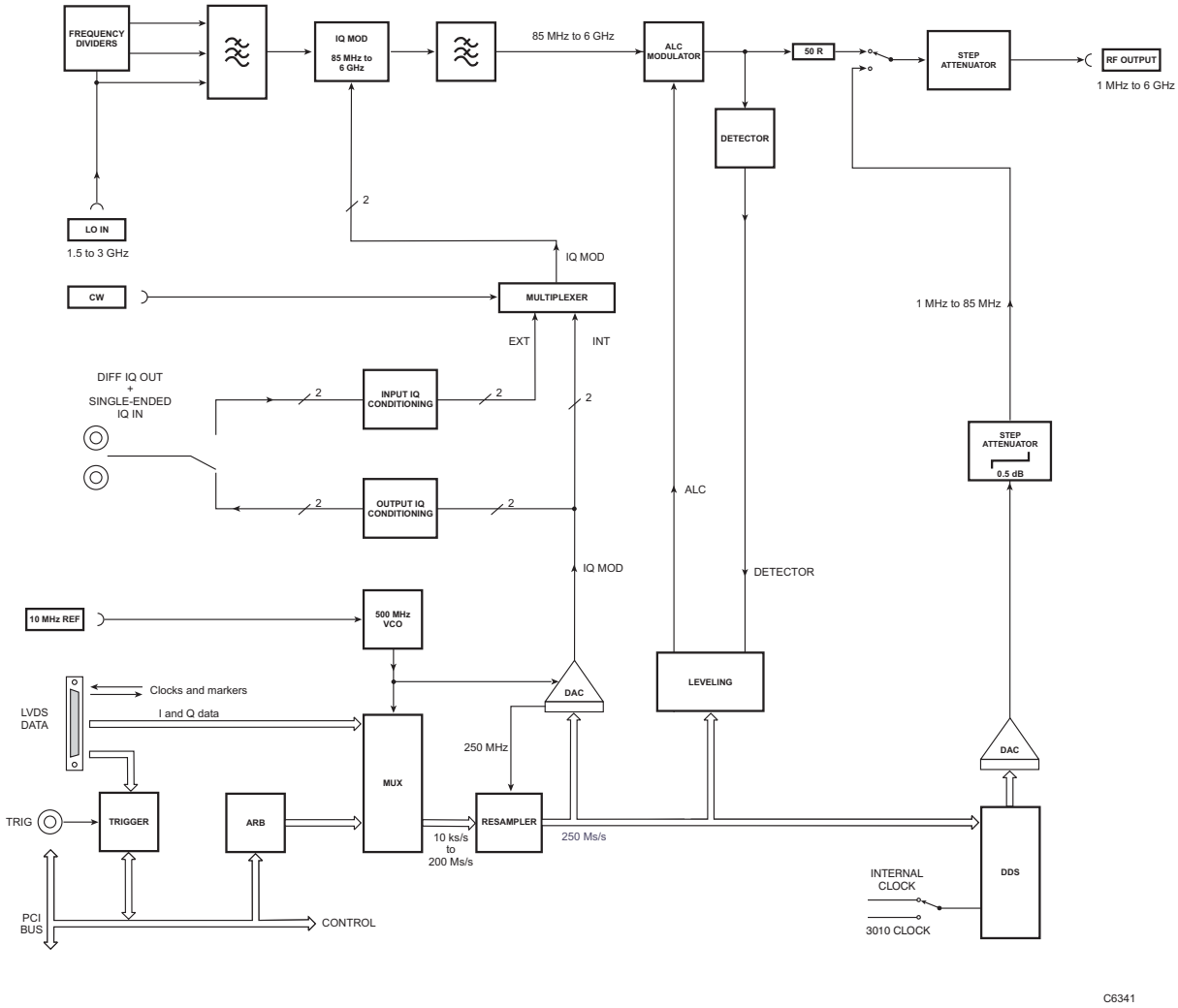


Fig. 22 3025C block schematic diagram

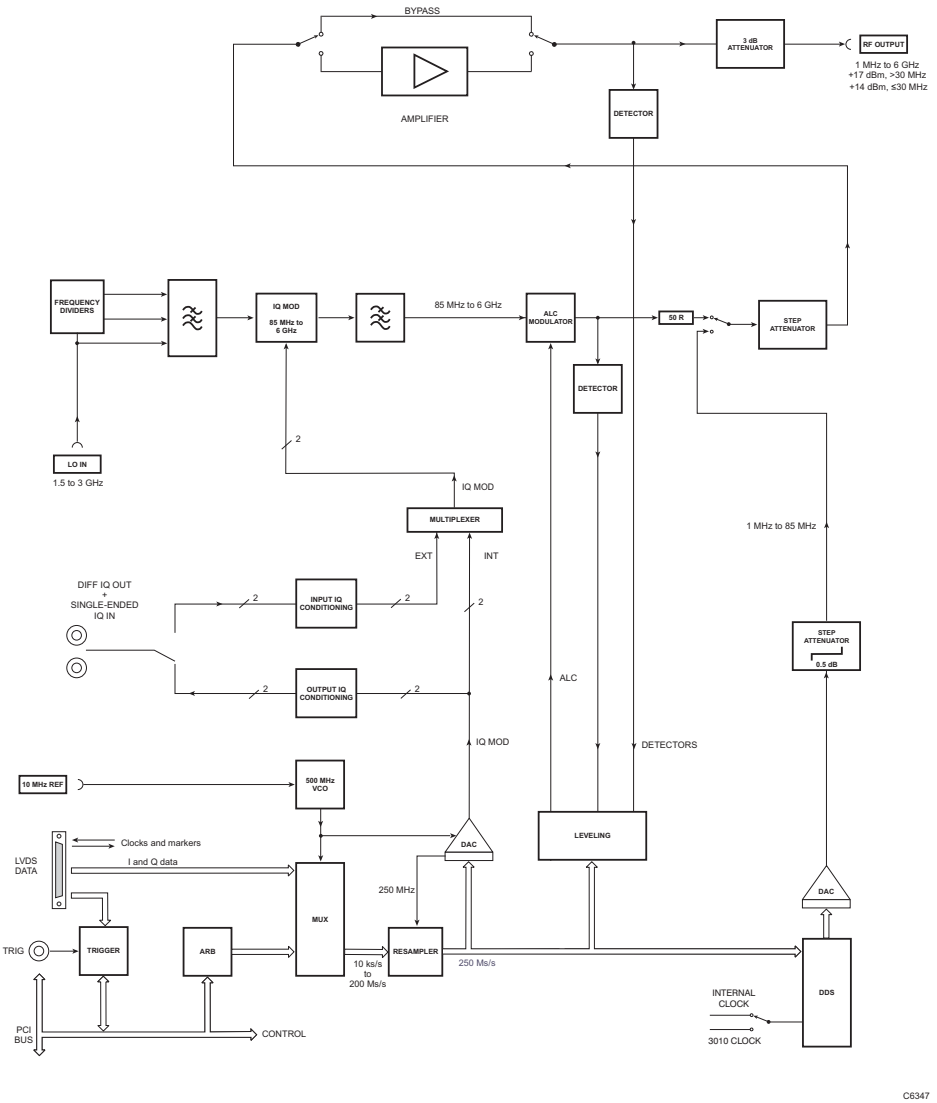


Fig. 23 3026C block schematic diagram

GLOSSARY

ACLR	Adjacent Channel Leakage Ratio: a measurement of transmitter performance for W-CDMA. It is the ratio of transmitted power to the power received (after filtering) in the adjacent RF channel. It describes the amount of distortion generated due to nonlinearities in RF components, and is a critical measurement for CDMA transmitters. Formerly called Adjacent Channel Power Ratio.
ACP(R)	See ACLR.
ADC	An Analog-to-Digital Converter converts a time-varying signal to discrete binary values.
AM	Amplitude Modulation: modulation of the amplitude of a carrier wave.
ARB	Arbitrary Waveform Generator: allows you to edit, generate and play complex recurring waveforms.
ATE	Automatic Test Equipment is program-controlled equipment that tests electronic devices for functionality and performance.
COM	Component Object Model: a way of implementing objects that can be used in environments different from the one they were created in, even across machine boundaries, and independently of language. COM allows the reuse of objects with no knowledge of their internal implementation, as well-defined interfaces are all that is visible to the user.
CW	Continuous Wave: electromagnetic waves, the successive oscillations of which are identical under steady-state conditions, which can be interrupted or modulated to convey information.
DAC	Digital-to-Analog Converter: device that converts a digital code to a time-varying analog signal.
dB	Decibel: a dimensionless logarithmic unit of measurement that expresses the ratio of a power relative to a specified or implied reference level.
dBc	Decibel value specified relative to the carrier level.
dBm	Decibels value specified relative to 1 mW.
DDS	Direct Digital Synthesis: producing an analog waveform — usually a sine wave — by generating a time-varying signal digitally and then performing a digital-to-analog conversion.

dll	dynamic link library: an executable file that allows programs to share code and other resources necessary to perform particular tasks.
EVM	Error Vector Magnitude is used to quantify the performance of a digital radio transmitter or receiver by measuring the deviation of received constellation points from their ideal positions.
FM	Frequency Modulation: modulation of the frequency of a carrier wave.
GND	Ground
GPIB	General Purpose Interface Bus: a parallel interface defined by the IEEE 488 standard, used for attaching sensors and programmable instruments to a computer.
GSM	Global System for Mobile communications: the first all-digital (2G) mobile network.
HF	High Frequency: radio signals in the range 3 MHz to 30 MHz.
IF	Intermediate Frequency: a frequency to which a carrier frequency is shifted as an intermediate step in superheterodyne transmission or reception.
IM(D)	Intermodulation (Distortion): the result of mixing different frequencies together, producing additional signals that are not generally harmonics of the originals.
IQ	In-phase/Quadrature modulation. A modulation scheme where a signal is modulated by two signals 90 degrees out of phase with each other.
LED	Light-Emitting Diode
LO	Local Oscillator**:** an electronic device used to generate a signal normally used to convert a signal of interest to a different frequency using a mixer. See IF.
LVDS	Low-Voltage Differential Signaling: uses a current source to transmit and receive fast signals over simple twisted-pair cable.
MF	Medium Frequency: radio signals in the range 300 kHz to 3 MHz.
PCI	Peripheral Component Interconnect
PM	Phase Modulation: the phase of a carrier is altered by the modulating signal.

PNP	Plug-'N'-Play
PXI	PCI eXtensions for Instrumentation
PXI Express	Backwards-compatible with PXI, but providing faster timing and signal lines.
QAM	Quadrature Amplitude Modulation: two amplitude-modulated carriers at the same frequency but at a relative phase angle of 90 degrees are combined in a single channel. This doubles the effective bandwidth of the transmission.
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RMS	Root Mean Square: the most common mathematical method of defining the effective voltage or current of an AC waveform.
SDRAM	Synchronous Dynamic RAM
SFP	Soft Front Panel: a representation of an instrument's control panel, generated in software, which allows you to control the underlying software and hardware.
SMA	SubMiniature version A (connector)
SMB	SubMiniature version B (connector)
TDMA	Time Division Multiple Access: a digital transmission technology that allows a number of users to access a single RF channel without interference by allocating unique time slots to each user within each channel.
TTL	Transistor-Transistor Logic: switching voltage ranges are V_{OL} = 0.4 V, V_{OH} = 2.4 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V
UHF	Ultra High Frequency: radio signals in the range 300 MHz to 3 GHz.
USB	Universal Serial Bus: a serial bus standard for connecting devices to a host computer, using a standardized interface socket and allowing devices to be connected and disconnected without removing power.

UUT	Unit Under Test
VCO	Voltage-Controlled Oscillator: a frequency generator whose output frequency is a function of an applied voltage. If the applied voltage varies, the output is modulated.
VHDCI	Very High Density Cable Interconnect
VHF	Very High Frequency: radio signals in the range 30 MHz to 300 MHz.
VSWR	Voltage Standing-Wave Ratio: the voltage ratio of the amplitude of a partial standing wave at an antinode (maximum) to the amplitude at an adjacent node (minimum), in a transmission line. A measure of the matching, and efficiency, of transmission devices.
VXI	VMEbus Extension for Instrumentation
WLAN	Wireless Local Area Network: a mobile user can connect to a local area network using a radio signal, over a short distance (usually indoors). Standard IEEE 802.11 defines the technology.
WMAN	Wireless Metropolitan Area Network: a mobile user can connect to a local area network using a radio signal, outdoors. Standard IEEE 802.16 defines the technology.